非隔离稳压单路 100A 输出，POL 数字模块电源



专利保护 RoHS

- 输入欠压、输出欠压/过压保护
- 输出过流、短路保护
- 过温保护

产品特点

- 小体积封装：25.4 x 12.7 x 14.5 mm
- 宽输入电压范围：7.5-14.4VDC
- 宽输出电压范围：0.5-2.5V
- 极小的输出电压偏差：±10 mV
- 极低的输出纹波和噪声：20 mVp-p
- 最大输出电流可高达 100A
- 效率可高达 93%
- 具有极小的负载动态变化：±50mV
- 宽工作温度范围：-40℃ to 85℃
- 可通过 PMBus 进行配置和监控
- 具备远端补偿功能

KD12T-100A 数字模块是非隔离 DC-DC 转换器，可提供高达 100A 的输出电流。该模块可满足 7.5 至 14.4VDC 的输入电压范围，并提供可调的精确的 0.5 至 2.5VDC 的输出电压，其输出电压可通过外部电阻分压或 PMBus 命令进行配置。该模块的功能还包括 PMBus 数字协议，远程 Enable，VR_RDY，过流，欠压，过压和过温保护。模块内部还包括一个实时补偿环路，用于优化动态响应以匹配负载跳变时的变化。该模块广泛应用于通信、计算机网络、电力分布式架构、工作站、服务器、局域网/广域网等领域，为 FPGA、DSP、ASIC 等高速芯片提供大电流瞬态响应快的稳定电压。

选型表

认证	产品型号	输入电压（VDC）	输出		输出电压偏差	输出电压纹波&噪声
		标称值（范围值）	电压（VDC）（范围值）	输出电流（A）最大值	（mV）最大值	（mVp-p）典型值
--	KD12T-100A	12（7.5-14.4）	0.5-2.5	100	±10	20

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目录

引脚说明 3
典型应用电路 4
极限额定值 5
产品电气特性 6
典型特征曲线 7
典型开关机波形 12
操作指南 13
外观尺寸图 26
载带包装示意图 27
PMBus 描述 28
PMBus 寄存器 34

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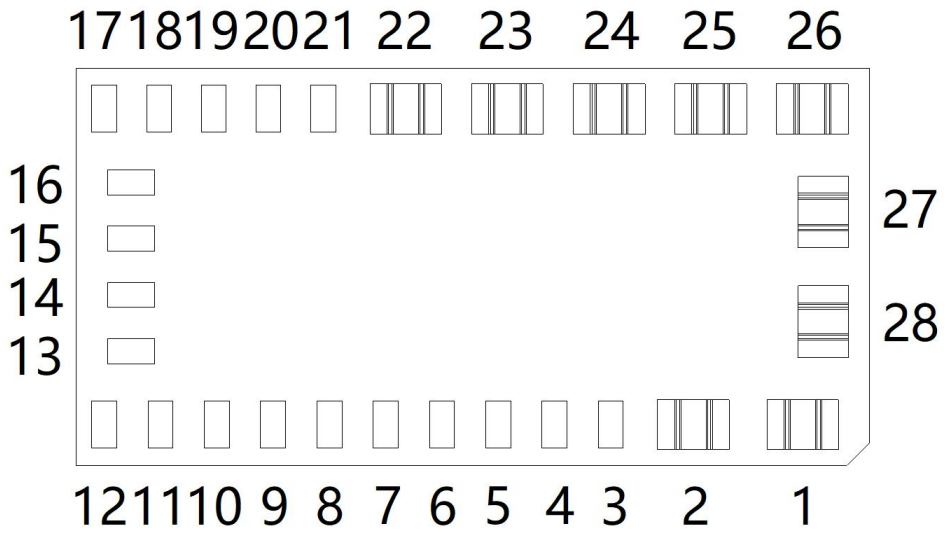
引脚说明



引脚布局的底部视图

引脚	符号	类型	功能
1, 28	VIN	Power	输入电压
2	GND	Power	输入电源地
22, 23 25, 26	VO	Power	电压输出
24, 27	GND	Power	输出电源地
3	VR_RDY	O	指示输出电压是否良好的开漏引脚, 可通过一个≥3kΩ的电阻上拉至 V3R3 引脚
4	V5	O	内部 LDO 的 5V 输入引脚，用于给内部逻辑电路供电
5	ENABLE	I	开启/关断模块的控制信号输入引脚
6	TSEN	I/O	连接智能功率模块的 TAO 引脚，用于采集外接的功率模块的温度
7	PWM3	O	第三通道的 PWM 信号输出，用于控制外接功率模块的 PWM 信号
8	PWM4	O	第四通道的 PWM 信号输出，用于控制外接功率模块的 PWM 信号
9	ADDR_TRISE	I	地址设置引脚
10	PMB_CLK	I	PMBus 时钟引脚
11	PMB_DIO	I/O	PMBus 数据引脚
12	PMB_ALERT#	O	PMBus ALERT 引脚
13	AGND	/	信号地
14	COMP	O	误差放大器输出
15	VREF	O	1.7V，500uA 内部稳压器基准电压，外接功率模块时需连接至 REFIN
16	NC	I	无功能引脚
17	VSP	I	输出电压远端检测正信号引脚
18	VSN	I	输出电压远端检测负信号引脚
19	V3R3	/	内部 LDO 的 3.3V 输出引脚
20	CSP3	I	第三通道的电流采集输入引脚，用于外接功率模块的电流采集
21	CSP4	I	第四通道的电流采集输入引脚，用于外接功率模块的电流采集

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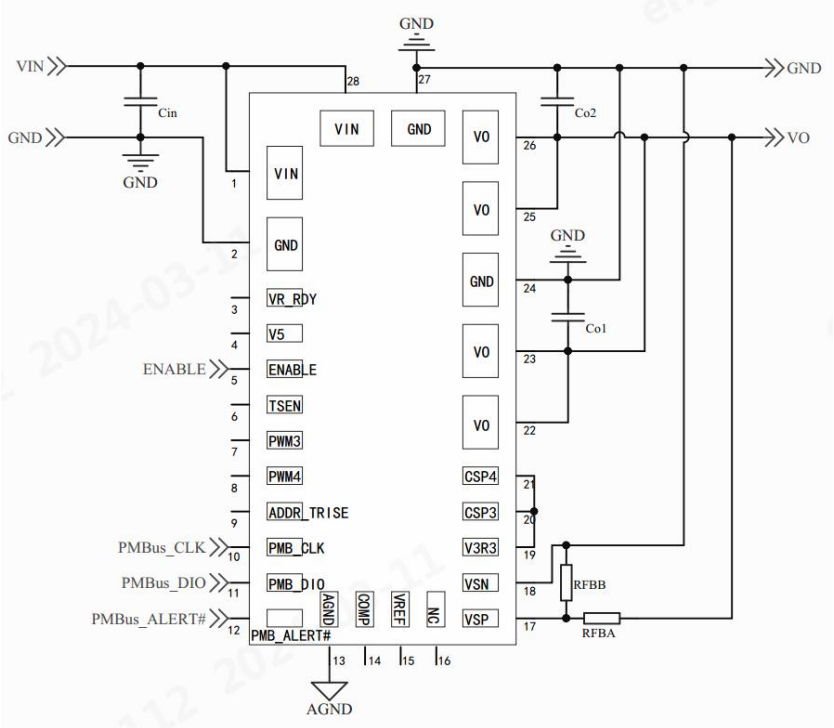
典型应用电路

单模块 100A 典型应用电路



Cin：3 x 470uF/10mΩ固态电解电容 + 10 x 10uF 陶瓷电容	RFBA、RFBB：用于调节输出电压
Co1：5 x 330uF/10mΩ铝电解电容 + 12 x 100uF 陶瓷电容	
Co2：5 x 330uF/10mΩ铝电解电容 + 12 x 100uF 陶瓷电容	

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极限额定值

		最小值	最大值	单位
电压	Vin	-0.3	19	V
	V5, TSEN, COMP	-0.3	6	V
	ADDR_TRISE, CSPx, ENABLE, PMB_CLK, PMB_DIO, PMB_ALERT#, V3R3, VSP, PWMx, VR_RDY	-0.3	3.6	V
	GND, VSN	-0.3	0.3	V
	VREF	-0.3	1.8	V
温度	工作温度 （详见温度降额曲线）	-40	+85	℃
	存储温度	-55	+125	℃
湿度	存储湿度（无凝结）	5	95	%RH
海拔高度		--	2000	m
回流焊温度	IPC/JEDEC J-STD-020D.1.	峰值温度 Tc≤245℃,217℃以上时间最大为 60 s		
潮敏等级	IPC/JEDEC J-STD-020D.1	MSL 3		
污染等级		PD 3		
振动		IEC/EN61373 - Category 1, Grade B		

注：
超出极限额定值可能会对模块造成永久性损坏，长时间暴露在极限额定值下会影响模块的可靠性。另外这些只是应力等级，并不意味着模块可以在极限额定值条件范围内进行功能操作。

配置文件

本产品采用数字控制电路设计，数字控制电路使用一个配置文件决定产品的功能和性能。除非另有说明，电气规格表显示的均为标准配置文件下的功能和性能规格值。标准配置文件可以适应大多数应用需求。在特定的应用中，可以更改标准配置文件以优化性能。其他应用如需更改配置文件，本技术手册规格仅作推荐使用。

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产品电气特性

以下部分规格与产品的数字控制相关，可用于可配置参数的 PMBus 命令已用大写字母标注。

若无特殊说明，以下规格的工作温度范围为-40 至+85℃，输入电压为 7.5 至 14.4 V，频率为 300KHz；以下规格的典型值的工作条件为工作温度 +25℃，输入电压 12.0 V，满载输出；另外输出电压需在引脚上测量，数字控制为标准配置文件。

另外需求外接 C_{IN} = 3 x 470 uF/10 mΩ OS-CON + 10 x 10 uF 陶瓷电容，C_{OUT} =10 x 330 uF/10 mΩ Polymer + 24 x 100 uF 陶瓷电容，如典型应用电路图。

规格	条件	最小值	典型值	最大值	单位
输入电压					
输入电压范围		7.5	12	14.4	V
输入电流					
输入空载电流	Vo = 0.85 V	--	110	--	mA
	Vo = 1.0 V	--	130	--	
	Vo = 1.2 V	--	170	--	
	Vo = 1.8 V	--	300	--	
	Vo = 2.5 V	--	490	--	
输出电压					
输出电压范围		0.5	--	2.5	V
输出电压精度		-10	0	10	mV
线性调整率		--	0	--	mV
负载调整率		--	0	--	
输出纹波&噪声（20MHz 带宽下）		--	20	--	mVp-p
瞬态响应偏差	标称输入电压，50%负载跳变	--	50	--	mV
输出电流					
输出电流		0	--	100	A
VREF					
VREF 基准电压	I_{VREF} = 0A	1.685	1.700	1.717	V
ENABLE					
ENABLE 高电平		1.0	---	3.0	V
ENABLE 低电平		0	---	0.3	V
ENABLE 关断时输入电流		---	---	1	mA
效率					
效率 max I_o	Vo = 0.85 V	--	85	--	%
	Vo = 1.0 V	--	85	--	
	Vo = 1.2 V	--	87	--	
	Vo = 1.8 V	--	91	--	
	Vo = 2.5 V	--	93	--	
MTBF					
平均无故障时间(MTBF)		--	6015801	--	hours
物理特性					
封装尺寸		25.4 x 12.7 x 14.5			mm
重量		--	13.5	--	g

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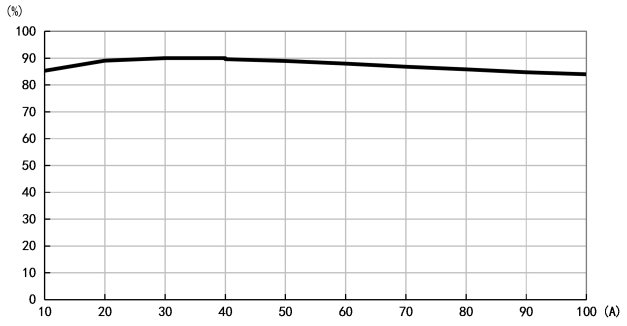
典型特征曲线

V_o = 0.85 V
除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

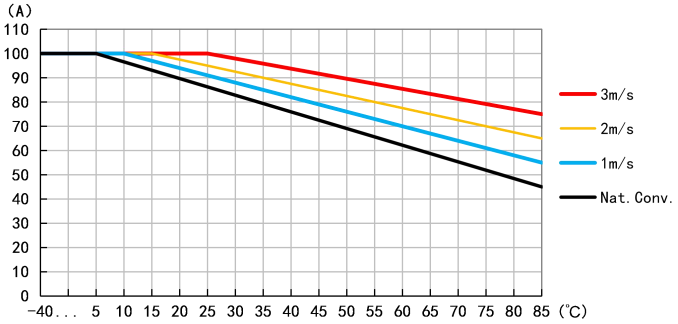
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

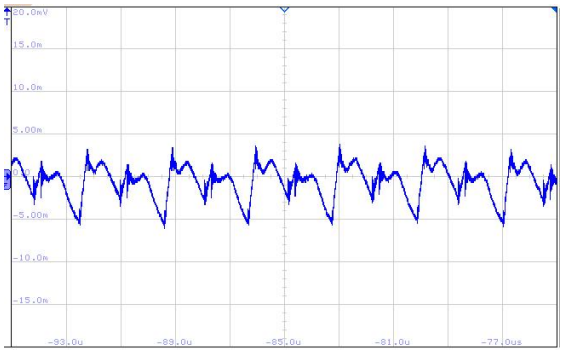


输出纹波和噪声

V_{in} = 12 V, I_o = 100 A,

C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

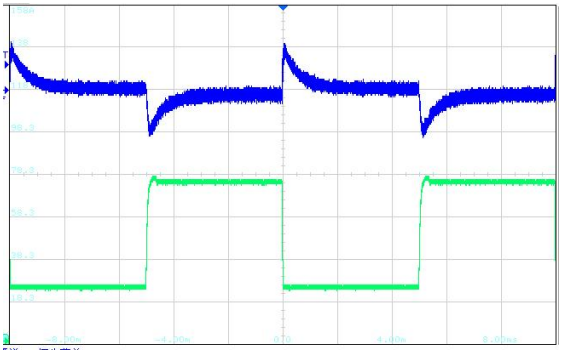


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in} = 12 V, C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 2ms/div.



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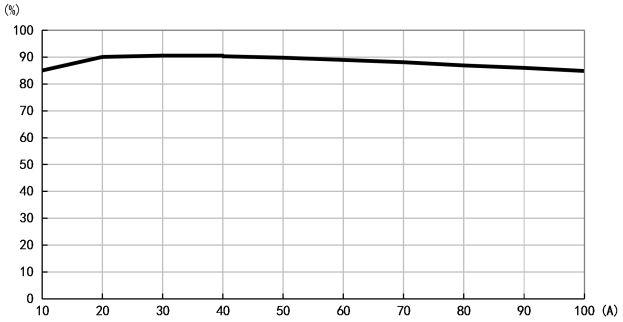
典型特征曲线

V_o = 1.0 V

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

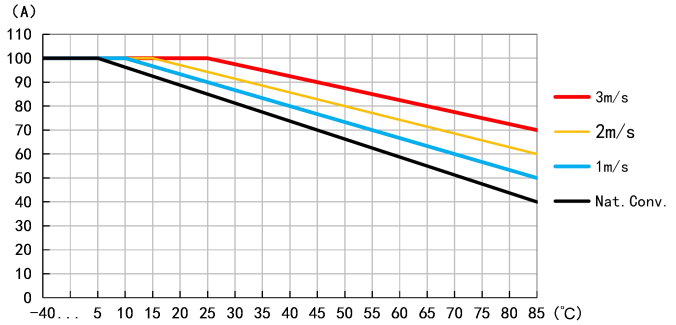
效率

效率 vs. 输出电流，V_{in} = 12V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

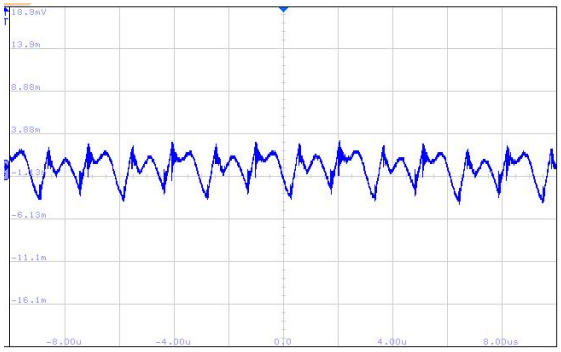


输出纹波和噪声

V_{in} = 12 V, I_o = 100 A,

C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

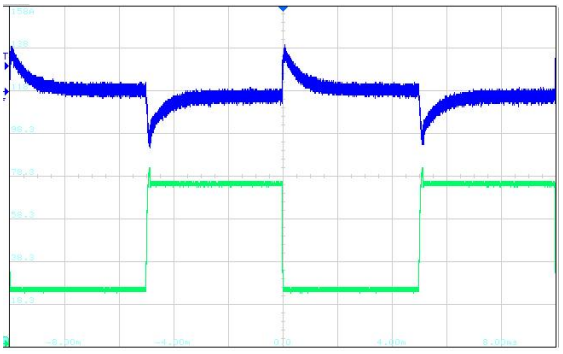


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 2ms/div.



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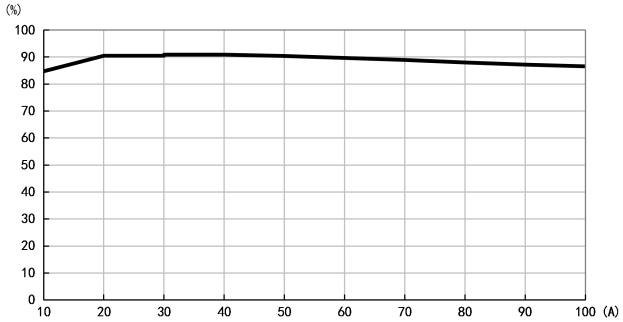
典型特征曲线

V_o = 1.2 V

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

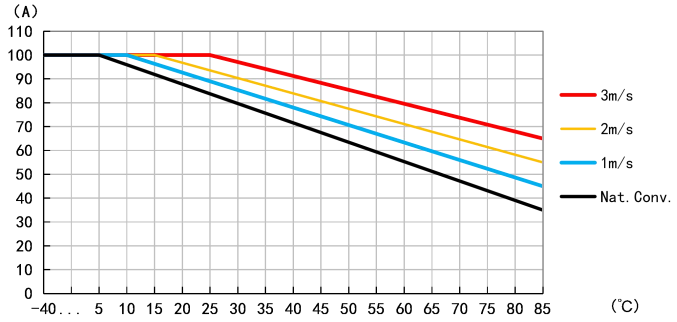
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

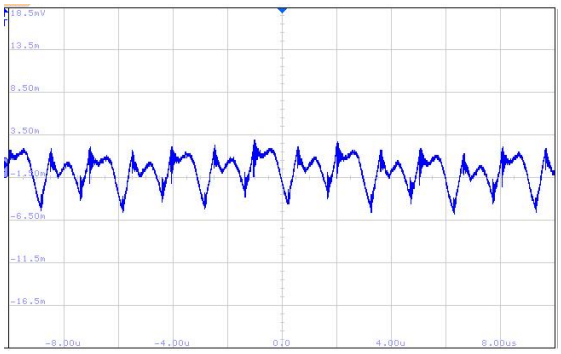


输出纹波和噪声

V_{in} = 12 V, I_o = 100 A,

C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

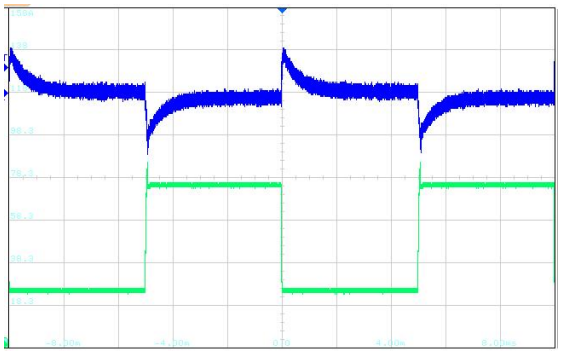


动态响应

输出电压动态响应，负载跳变（25% - 75% - 25%）

V_{in} = 12 V, C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 2ms/div.



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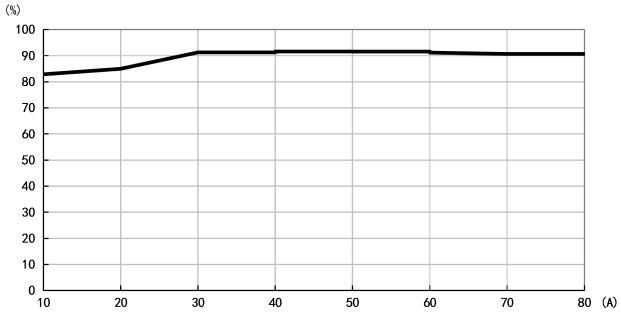
典型特征曲线

V_o = 1.8 V

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

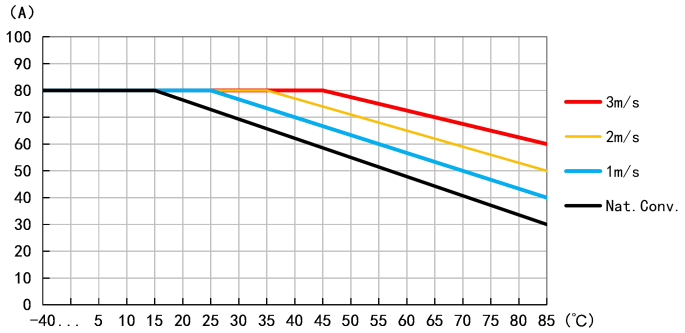
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

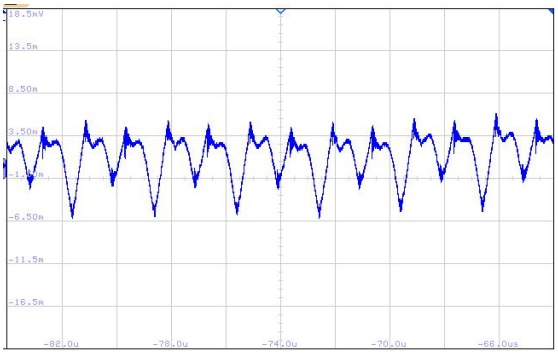


输出纹波和噪声

V_{in} = 12 V, I_o = 100 A,

C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

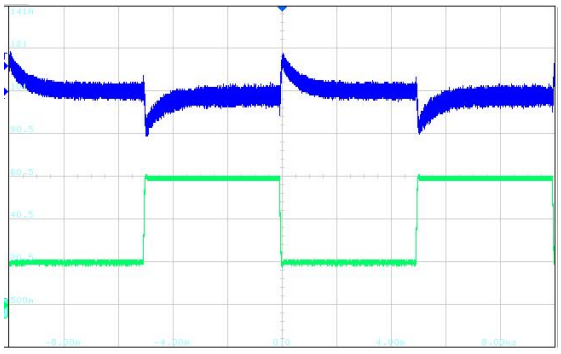


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in} = 12 V, C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 2ms/div.



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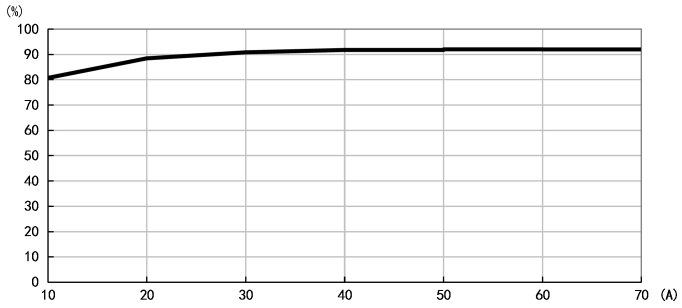
典型特征曲线

V_o = 2.5 V

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

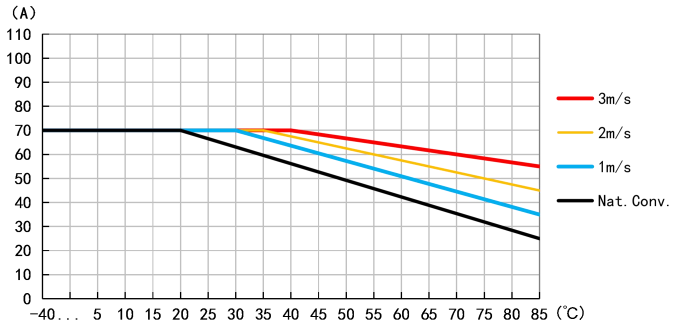
效率

效率 vs. 输出电流，V_{in} = 12 V



温度降额曲线

负载电流 vs. 环境温度和风速，V_{in} = 12 V

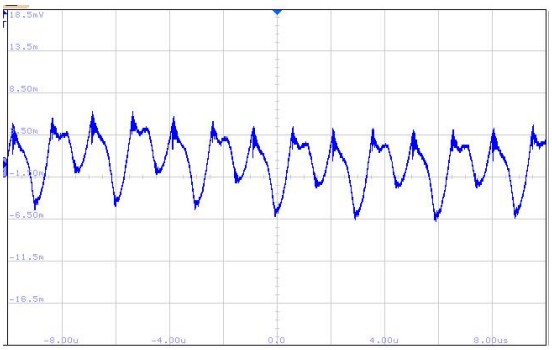


输出纹波和噪声

V_{in} = 12 V, I_o = 100 A,

C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF

示波器坐标轴：5 mV/div, 2 μs/div, 20 MHz 带宽.

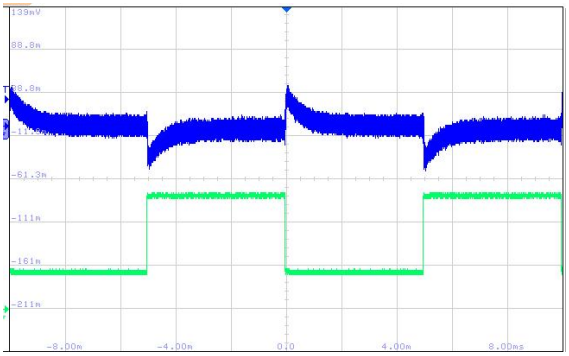


动态响应

输出电压动态响应，负载跳变（25%－75%－25%）

V_{in} = 12 V, C_{OUT} = 10 x 330 μF/10 mΩ + 24 x 100 μF, di/dt = 2 A/μs,

示波器坐标轴：50 mV/div, 20 A/div, 2 ms/div.



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典型开关机波形

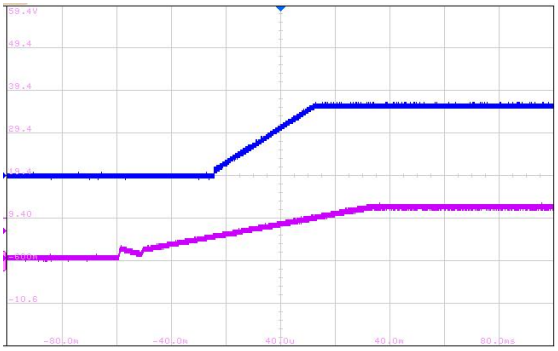
V_o = 0.85 V

除非另有说明，以下波形工作条件为：工作温度+25℃，标准配置文件下。

开机波形

V_{in} = 12 V, I_o = 100 A.

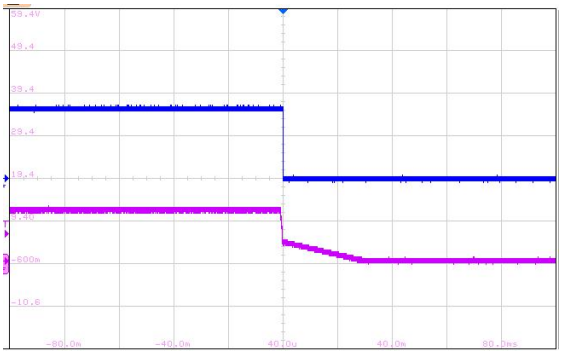
示波器坐标轴：0.5V/div（Vo：蓝色），10 V/div（Vin：紫色），20 ms/div.



关机波形

V_{in} = 12 V, I_o = 100 A.

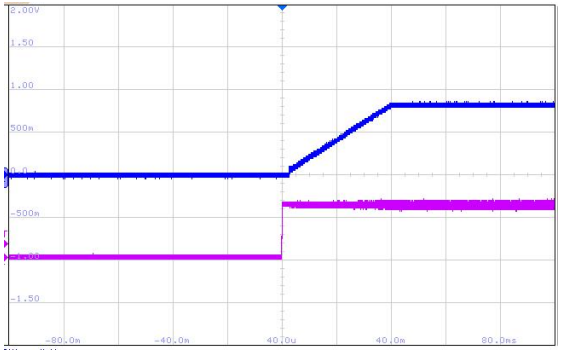
示波器坐标轴：0.5V/div（Vo：蓝色），10 V/div（Vin：紫色），20 ms/div.



ENABLE 开启波形

V_{in} = 12 V, I_o = 100 A.

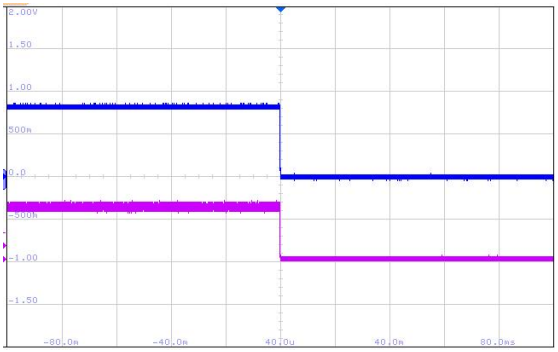
示波器坐标轴：0.5V/div（Vo：蓝色），2 V/div（ENABLE：紫色），20 ms/div.



ENABLE 关断波形

V_{in} = 12 V, I_o = 100 A.

示波器坐标轴：0.5V/div（Vo：蓝色），2 V/div（ENABLE：紫色），20 ms/div.



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操作指南

动态过冲调节（OSR 以及 USR）

OSR：当输出负载动态减少时，输出电压产生动态过冲，当过冲幅度超过设定的 OSR 值时，模块内部 PWMx 立即变为三态模式，三态模式下会关闭高侧和低侧 MOS，此时电感上的能量会被低侧 MOS 的体二极管耗散，此方法可用于降低动态负载时产生的输出电压过冲值。

USR：当输出负载动态增加时，输出电压产生动态欠冲，当欠冲幅度超过设定的 USR 值时，模块内部 PWMx 会增加脉冲，以更快速的提供负载能量。

MFR_SPEC_09[2:0]用于设置 OSR 幅值，MFR_SPEC_09[6:4]用于设置 USR 幅值，如下表：

动态过冲调节（OSR 以及 USR）			Min.	Typ.	Max.	单位
V_{OSR}	OSR 幅值设置	MFR_SPEC_09[2:0]=000b	20	30	40	mV
		MFR_SPEC_09[2:0]=001b	30	40	50	
		MFR_SPEC_09[2:0]=010b	50	60	70	
		MFR_SPEC_09[2:0]=011b	70	80	90	
		MFR_SPEC_09[2:0]=100b	90	100	110	
		MFR_SPEC_09[2:0]=101b	110	120	130	
		MFR_SPEC_09[2:0]=110b	130	140	150	
		MFR_SPEC_09[2:0]=111b	关断 OSR 功能			
V_{USR}	USR 幅值设置	MFR_SPEC_09[6:4]=000b	10	20	30	mV
		MFR_SPEC_09[6:4]=001b	20	30	40	
		MFR_SPEC_09[6:4]=010b	50	60	70	
		MFR_SPEC_09[6:4]=011b	70	80	90	
		MFR_SPEC_09[6:4]=100b	90	100	110	
		MFR_SPEC_09[6:4]=101b	110	120	130	
		MFR_SPEC_09[6:4]=110b	130	140	150	
		MFR_SPEC_09[6:4]=111b	关断 USR 功能			
V_{OSRHYS}	OSR 回差		--	10	--	mV
V_{USRHYS}	USR 回差		--	10	--	mV

电流共享均流平衡

电流共享均流的机制是通过监测每一相的平均电流，然后调节每一相的 PWM 脉宽，使每一相的电流均衡。模块内部通过监测 CSPn 电压，并比较每个 CSPn 在 5us 内的平均值，当第 n 相的 CSPn＞CSP 平均值（每相 CSP 电压取和后平均）时，就会缩短 PWMn 的脉宽，以减少第 n 相的电流；当其中一相的 CSPn＜CSP 平均值时，就会增加 PWMn 的脉宽，以增加第 n 相的电流，以实现电流均衡。

相位重叠限制

在稳态工作下，每相的导通脉冲不能重叠，这个机制限制了应用的占空比，模块的占空比不能超过 1/n。但模块允许在瞬态期间，即 USR 触发期间出现相位重叠。

输出电压调节

输出电压调节可采用两种方法：

VID 数字调节输出电压：参考以下两个表格配置 VID code，其中 VID 有两个模式，分别为 VR12.0 和 VR12.5，这两个模式可通过 MFR_SPECIFIC_13:[7]

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设置。另外输出电压还可以通过 MFR_SPECIFIC_05 进行 TRIM 微调。

VID 数字调节			Min.	Typ.	Max.	单位
V_{VIDSTP}	输出电压可调步进	VR12.5	--	10	--	mV
		VR12.0	--	5	--	
V_{BOOT}	BOOT 电压设置（B0）	$R_{ADDR-TRISE}$=24kΩ/39kΩ/75kΩ	--	1	--	
		$R_{ADDR-TRISE}$≤20kΩ	--	0	--	
	BOOT 电压设置（$B_3B_2B_1$）	MFR_SPEC_11[3:1]=000b	000			
		MFR_SPEC_11[3:1]=001b	001			
		MFR_SPEC_11[3:1]=010b	010			
		MFR_SPEC_11[3:1]=011b	011			
		MFR_SPEC_11[3:1]=100b	100			
		MFR_SPEC_11[3:1]=101b	101			
		MFR_SPEC_11[3:1]=110b	110			
		MFR_SPEC_11[3:1]=111b	111			
	BOOT 电压设置（$B_7B_6B_5B_4$）	MFR_SPEC_11[7:4]=0000b	0000			
		MFR_SPEC_11[7:4]=0001b	0001			
		MFR_SPEC_11[7:4]=0010b	0010			
		MFR_SPEC_11[7:4]=0011b	0011			
		MFR_SPEC_11[7:4]=0100b	0100			
		MFR_SPEC_11[7:4]=0101b	0101			
		MFR_SPEC_11[7:4]=0110b	0110			
		MFR_SPEC_11[7:4]=0111b	0111			
		MFR_SPEC_11[7:4]=1000b	1000			
		MFR_SPEC_11[7:4]=1001b	1001			
		MFR_SPEC_11[7:4]=1010b	1010			
		MFR_SPEC_11[7:4]=1011b	1011			
		MFR_SPEC_11[7:4]=1100b	1100			
		MFR_SPEC_11[7:4]=1101b	1101			
		MFR_SPEC_11[7:4]=1110b	1110			
		MFR_SPEC_11[7:4]=1111b	1111			

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VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
00	0	0
01	0.25	0.50
02	0.255	0.51
03	0.26	0.52
04	0.265	0.53
05	0.27	0.54
06	0.275	0.55
07	0.28	0.56
08	0.285	0.57
09	0.29	0.58
0A	0.295	0.59
0B	0.30	0.60
0C	0.305	0.61
0D	0.31	0.62
0E	0.315	0.63
0F	0.32	0.64
10	0.325	0.65
11	0.33	0.66
12	0.335	0.67
13	0.34	0.68
14	0.345	0.69
15	0.35	0.70
16	0.355	0.71
17	0.36	0.72
18	0.365	0.73
19	0.37	0.74
1A	0.375	0.75
1B	0.38	0.76
1C	0.385	0.77
1D	0.39	0.78
1E	0.395	0.79
1F	0.40	0.80
20	0.405	0.81
21	0.41	0.82

VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
22	0.415	0.83
23	0.42	0.84
24	0.425	0.85
26	0.43	0.86
56	0.435	0.87
27	0.44	0.88
28	0.445	0.89
29	0.45	0.90
2A	0.455	0.91
2B	0.46	0.92
2C	0.465	0.93
2D	0.47	0.94
2E	0.475	0.95
2F	0.48	0.96
30	0.485	0.97
31	0.49	0.98
32	0.495	0.99
33	0.50	1.00
34	0.505	1.01
35	0.51	1.02
36	0.515	1.03
37	0.52	1.04
38	0.525	1.05
39	0.53	1.06
3A	0.535	1.07
3B	0.54	1.08
3C	0.545	1.09
3D	0.55	1.10
3E	0.555	1.11
3F	0.56	1.12
40	0.565	1.13
41	0.57	1.14
42	0.575	1.15
43	0.58	1.16

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VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
44	0.585	1.17
45	0.59	1.18
46	0.595	1.19
47	0.60	1.20
48	0.605	1.21
49	0.61	1.22
4A	0.615	1.23
4B	0.62	1.24
4C	0.625	1.25
4D	0.63	1.26
4E	0.635	1.27
4F	0.64	1.28
50	0.645	1.29
51	0.65	1.30
52	0.655	1.31
53	0.66	1.32
54	0.665	1.33
55	0.67	1.34
56	0.675	1.35
57	0.68	1.36
58	0.685	1.37
59	0.69	1.38
5A	0.695	1.39
5B	0.70	1.40
5C	0.705	1.41
5D	0.71	1.42
5E	0.715	1.43
5F	0.72	1.44
60	0.725	1.45
61	0.73	1.46
62	0.735	1.47
63	0.74	1.48
64	0.745	1.49
65	0.75	1.50

VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
66	0.755	1.51
67	0.76	1.52
68	0.765	1.53
69	0.77	1.54
6A	0.775	1.55
6B	0.78	1.56
6C	0.785	1.57
6D	0.79	1.58
6E	0.795	1.59
6F	0.80	1.60
70	0.805	1.61
71	0.81	1.62
72	0.815	1.63
73	0.82	1.64
74	0.825	1.65
75	0.83	1.66
76	0.835	1.67
77	0.84	1.68
78	0.845	1.69
79	0.85	1.70
7A	0.855	1.71
7B	0.86	1.72
7C	0.865	1.73
7D	0.87	1.74
7E	0.875	1.75
7F	0.88	1.76
80	0.885	1.77
81	0.89	1.78
82	0.895	1.79
83	0.90	1.80
84	0.905	1.81
85	0.91	1.82
86	0.915	1.83
87	0.92	1.84

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VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
88	0.925	1.85
89	0.93	1.86
8A	0.935	1.87
8B	0.94	1.88
8C	0.945	1.89
8D	0.95	1.90
8E	0.955	1.91
8F	0.96	1.92
90	0.965	1.93
91	0.97	1.94
92	0.975	1.95
93	0.98	1.96
94	0.985	1.97
95	0.99	1.98
96	0.995	1.99
97	1.00	2.00
98	1.005	2.01
99	1.01	2.02
9A	1.015	2.03
9B	1.02	2.04
9C	1.025	2.05
9D	1.03	2.06
9E	1.035	2.07
9F	1.04	2.08
A0	1.045	2.09
A1	1.05	2.10
A2	1.055	2.11
A3	1.06	2.12
A4	1.065	2.13
A5	1.07	2.14
A6	1.075	2.15
A7	1.08	2.16
A8	1.085	2.17
A9	1.09	2.18

VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
AA	1.095	2.19
AB	1.10	2.20
AC	1.105	2.21
AD	1.11	2.22
AE	1.115	2.23
AF	1.12	2.24
B0	1.125	2.25
B1	1.13	2.26
B2	1.135	2.27
B3	1.14	2.28
B4	1.145	2.29
B5	1.15	2.30
B6	1.155	2.31
B7	1.16	2.32
B8	1.165	2.33
B9	1.17	2.34
BA	1.175	2.35
BB	1.18	2.36
BC	1.185	2.37
BD	1.19	2.38
BE	1.195	2.39
BF	1.20	2.40
C0	1.205	2.41
C1	1.21	2.42
C2	1.215	2.43
C3	1.22	2.44
C4	1.225	2.45
C5	1.23	2.46
C6	1.235	2.47
C7	1.24	2.48
C8	1.245	2.49
C9	1.25	2.50
CA	1.255	N/A
CB	1.26	N/A

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VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
CC	1.265	N/A
CD	1.27	N/A
CE	1.275	N/A
CF	1.28	N/A
D0	1.285	N/A
D1	1.29	N/A
D2	1.295	N/A
D3	1.30	N/A
D4	1.305	N/A
D5	1.31	N/A
D6	1.315	N/A
D7	1.32	N/A
D8	1.325	N/A
D9	1.33	N/A
DA	1.335	N/A
DB	1.34	N/A
DC	1.345	N/A
DD	1.35	N/A
DE	1.355	N/A
DF	1.36	N/A
E0	1.365	N/A
E1	1.37	N/A
E2	1.375	N/A
E3	1.38	N/A
E4	1.385	N/A
E5	1.39	N/A
E6	1.395	N/A
E7	1.40	N/A
E8	1.405	N/A
E9	1.41	N/A
EA	1.415	N/A
EB	1.42	N/A
EC	1.425	N/A
ED	1.43	N/A

VID Hex VALUE	VR12.0 VOLTAGE(V)	VR12.5 VOLTAGE(V)
EE	1.435	N/A
EF	1.44	N/A
F0	1.445	N/A
F1	1.45	N/A
F2	1.455	N/A
F3	1.46	N/A
F4	1.465	N/A
F5	1.47	N/A
F6	1.475	N/A
F7	1.48	N/A
F8	1.485	N/A
F9	1.49	N/A
FA	1.495	N/A
FB	1.50	N/A
FC	1.505	N/A
FD	1.51	N/A
FE	1.515	N/A
FF	1.52	N/A

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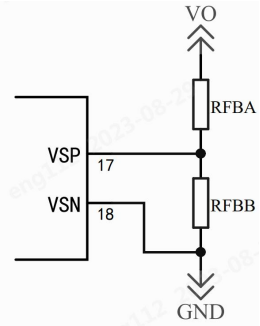
VID 数字调节输出电压时，还可以设置其转换速率，可参考下表：

VID 电压转换速率			Min.	Typ.	Max.	单位
SL_{SET}	VID 电压转换速率设置	MFR_SPEC_13[2:0]=000b 且 MFR_SPEC_07[2]=0b	0.28	0.34	--	mV/us
		MFR_SPEC_13[2:0]=001b 且 MFR_SPEC_07[2]=0b	0.60	0.68	--	
		MFR_SPEC_13[2:0]=010b 且 MFR_SPEC_07[2]=0b	0.91	1.02	--	
		MFR_SPEC_13[2:0]=011b 且 MFR_SPEC_07[2]=0b	1.22	1.36	--	
		MFR_SPEC_13[2:0]=100b 且 MFR_SPEC_07[2]=0b	1.53	1.70	--	
		MFR_SPEC_13[2:0]=101b 且 MFR_SPEC_07[2]=0b	1.85	2.04	--	
		MFR_SPEC_13[2:0]=110b 且 MFR_SPEC_07[2]=0b	2.16	2.38	--	
		MFR_SPEC_13[2:0]=111b 且 MFR_SPEC_07[2]=0b	2.48	2.74	--	
		MFR_SPEC_13[2:0]=000b 且 MFR_SPEC_07[2]=1b	1.53	1.70	--	
		MFR_SPEC_13[2:0]=001b 且 MFR_SPEC_07[2]=1b	1.85	2.04	--	
		MFR_SPEC_13[2:0]=010b 且 MFR_SPEC_07[2]=1b	2.16	2.38	--	
		MFR_SPEC_13[2:0]=011b 且 MFR_SPEC_07[2]=1b	2.48	2.74	--	
		MFR_SPEC_13[2:0]=100b 且 MFR_SPEC_07[2]=1b	2.79	3.08	--	
		MFR_SPEC_13[2:0]=101b 且 MFR_SPEC_07[2]=1b	3.10	3.43	--	
		MFR_SPEC_13[2:0]=110b 且 MFR_SPEC_07[2]=1b	3.41	3.76	--	
		MFR_SPEC_13[2:0]=111b 且 MFR_SPEC_07[2]=1b	3.73	4.13	--	

VSP 电压模拟调节：

模块引脚的 VSP 和 VSN 用于远端补偿，模块会使 VSP 以及 VSN 之间的电压稳定在 VID code 设定的输出电压，可以通过分压电阻实现输出电压的调节，如下图：



可通过以下公式选择 R_{FBA} 以及 R_{FBB} 的阻值：

$$V_{OUT} = \frac{V_{VID} \times (R_{FBA} + R_{FBB})}{R_{FBB}}$$

注：

1. 使用 VSP 电压模拟调节时，R_{FBA} 以及 R_{FBB} 均需连接在远端处，用于远端补偿。

2. KD12T-100A 读取的输出电压值为 VSP 与 VSN 之间的电压，当采用 VSP 电压模拟调节的方法时，读取的值与实际的输出电压不一致。

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输入欠压保护（UVLO）

KD12T-100A 通过 VIN 引脚连续监测输入电压，当输入电压低于 UVLO 阈值时，模块关断。输入电压高于 UVLO 阈值时，模块重启，回差为 1.05V。

另外 KD12T-100A 还会监测 V5 电压，如果 V5 电压低于 4.05V 时，模块关断，如果 V5 电压回升至 4.25V 时，模块则重新打开。

VIN UVLO 设置	欠压开启点(V)	欠压关断点(V)
MFR_SPEC_16[1:0]=00	4.5	3.5
MFR_SPEC_16[1:0]=01	7.25	6.25
MFR_SPEC_16[1:0]=10	9.0	8.0
MFR_SPEC_16[1:0]=11	10.3	9.3

输出欠压保护（UVP）

KD12T-100A 模块的输出欠压保护为跟踪值，当输出电压降低至 V_{VID}-V_{RDYL}，模块 PWM 将输出 1.7V，关断高低侧 MOS，并在 22ms 打嗝延迟后，模块尝试重新启动，如果 UVP 故障未消除，则会重复以上动作。其中输出欠压阈值 V_{RDYL} 可通过 MFR_SPECIFIC_22 设置。

注：UVP 保护检测的是 VSP 以及 VSN 之间的电压。

UVP 设置	V_{RDYL}(mV)
MFR_SPEC_22[2:0]=000	50
MFR_SPEC_22[2:0]=001	100
MFR_SPEC_22[2:0]=010	150
MFR_SPEC_22[2:0]=011	200
MFR_SPEC_22[2:0]=100	250
MFR_SPEC_22[2:0]=101	300
MFR_SPEC_22[2:0]=110	325
MFR_SPEC_22[2:0]=111	400

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输出过压保护（OVP）

KD12T-100A 有三重输出过压保护：

输出过压跟踪值：当输出电压大于 $V_{VID}+V_{OVPT5}$(VR12.5)/$V_{VID}+V_{OVPT0}$(VR12.0)时，触发输出过压保护。该保护阈值在 VID 电压更改时或 ENABLE 处于低电平时不生效。触发该阈值后，模块会将 VR_RDY 拉低并将所有 PWMx 输出至低电平，从而打开低侧 MOS 以放电输出电压，直到 ENABLE/VIN 切换。

输出过压固定值：当输出电压大于 V_{OVPF5}（VR12.5）/V_{OVPF0}（VR12.0）时，触发输出过压保护。该保护阈值可在 VID 电压更改时持续生效，但在 ENABLE 处于低电平时依旧不生效。触发该阈值后，模块会将 VR_RDY 拉低并将所有 PWMx 输出至低电平，从而打开低侧 MOS 以放电输出电压，直到 ENABLE/VIN 切换。

输出过压预偏置值：当输出电压大于 V_{OVPFP}时，触发输出过压保护。该保护阈值在 ENABLE 处于低电平时也可以生效。触发该阈值后，模块会将 VR_RDY 拉低并将所有 PWMx 输出至低电平，从而打开低侧 MOS 以放电输出电压，直到 VIN 切换。

注：OVP 保护检测的是 VSP 以及 VSN 之间的电压。

输出过压保护			Min.	Typ.	Max.	单位
V_{OVPFP}	输出过压预偏置值	ENABLE 低电平，V_{VSP} ＞V_{OVPFP}	--	2.75	--	V
V_{OVPF5}	输出过压固定值（VR.12.5）	ENABLE 高电平，(V_{VSP} - V_{VSN})＞V_{OVPF5}，1us，V_{OUT}≤1.8V	--	2.2	--	V
		ENABLE 高电平，(V_{VSP} - V_{VSN})＞V_{OVPF5}，1us，1.8V＜V_{OUT}≤2.0V	--	2.4	--	V
		ENABLE 高电平，(V_{VSP} - V_{VSN})＞V_{OVPF5}，1us，2.0V＜V_{OUT}≤2.2V	--	2.6	--	V
		ENABLE 高电平，(V_{VSP} - V_{VSN})＞V_{OVPF5}，1us，V_{OUT}＞2.2V	--	2.8	--	V
V_{OVPF0}	输出过压固定值（VR.12.0）	ENABLE 高电平，(V_{VSP} - V_{VSN})＞V_{OVPF0}，1us	1.7	1.75	1.8	V
V_{OVPT5}	输出过压跟踪值（VR.12.5）	测量 VSP 引脚，模块锁存	340	375	405	mV
V_{OVPT0}	输出过压跟踪值（VR.12.0）	测量 VSP 引脚，模块锁存	200	225	250	mV

输出过流限制（OCL）以及输出过流保护（OCP）

KD12T-100A 可通过 MFR_SPEC_00[3:0]设置每相的输出过流阈值。当触发输出过流阈值时，模块会延迟下一个 ON 脉冲的产生，直到电流降至输出过流阈值以下，此时输出电压由于没有 ON 脉冲，会持续的下降直至触发 UVP。

MFR_SPEC_00[3:0]设置每相的输出过流阈值可参考下表：

输出过流保护			Min.	Typ.	Max.	单位
I_{OCLX}	每相的过流阈值，V_{CSPx}-VREF，谷值电流限制	MFR_SPEC_00[3:0]=0000b	21	24	27	A
		MFR_SPEC_00[3:0]=0001b	25	27	30	
		MFR_SPEC_00[3:0]=0010b	28	30	33	
		MFR_SPEC_00[3:0]=0011b	31	33	36	
		MFR_SPEC_00[3:0]=0100b	34	36	39	
		MFR_SPEC_00[3:0]=0101b	37	39	42	
		MFR_SPEC_00[3:0]=0110b	40	42	45	
		MFR_SPEC_00[3:0]=0111b	43	45	48	
		MFR_SPEC_00[3:0]=1000b	46	48	51	
		MFR_SPEC_00[3:0]=1001b	49	51	54	
		MFR_SPEC_00[3:0]=1010b	52	54	57	

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		MFR_SPEC_00[3:0]=1011b	55	57	60	
		MFR_SPEC_00[3:0]=1100b	58	60	63	
		MFR_SPEC_00[3:0]=1101b	61	63	66	
		MFR_SPEC_00[3:0]=1110b	64	66	69	
		MFR_SPEC_00[3:0]=1111b	67	69	72	

另外 KD12T-100A 还可设置总电流（所有相位电流的总和）的过流限制阈值，当总电流高于过流限制阈值时，模块会关闭高低侧 MOS 并进入打嗝模式，直到过流状态消除，过流限制阈值可通过 OC_FAULT_LIMIT 设置。

过温保护（OTP）

当 KD12T-100A 模块通过 TSEN 引脚检测到的温度高于过温故障阈值 OTP_{THLD} 时，模块将关闭高低侧 MOS，当温度降低至过温阈值-15℃时，模块将重新启动。

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工作频率

KD12T-100A 模块的工作频率可通过 MFR_SPEC_12[7:4]设置，具体可参考下表：

注：KD12T-100A 的工作频率是准固定频率，其 ON 时间是根据输入电压(VIN 引脚采集的电压)和输出电压（V_{VID}）固定的。OFF 时间时根据负载、智能功率模块等各种因素而变化的。

开关频率			Min.	Typ.	Max.	单位
f_{SW}	开关频率	MFR_SPEC_12[7:4]=0000b	270	300	330	kHz
		MFR_SPEC_12[7:4]=0001b	360	400	440	
		MFR_SPEC_12[7:4]=0010b	450	500	550	
		MFR_SPEC_12[7:4]=0011b	540	600	660	
		MFR_SPEC_12[7:4]=0100b	630	700	770	
		MFR_SPEC_12[7:4]=0101b	720	800	880	
		MFR_SPEC_12[7:4]=0110b	810	900	990	
		MFR_SPEC_12[7:4]=0111b	900	1000	1100	
		MFR_SPEC_12[7:4]=1000b	315	350	385	
		MFR_SPEC_12[7:4]=1001b	405	450	495	
		MFR_SPEC_12[7:4]=1010b	495	550	605	
		MFR_SPEC_12[7:4]=1011b	585	650	715	
		MFR_SPEC_12[7:4]=1100b	675	750	825	
		MFR_SPEC_12[7:4]=1101b	765	850	935	
		MFR_SPEC_12[7:4]=1110b	855	950	1045	
		MFR_SPEC_12[7:4]=1111b	900	1000	1100	

软启动时间

KD12T-100A 模块的软启动时间可通过 MFR_SPEC_12[1:0]设置，具体可参考下表：

注：$R_{ADDR-TRISE}$还会影响到 VID 电压的设置以及地址位的设置，详情可查阅 **VID 数字调节输出电压**以及 **PMBus 地址位**。

软启动时间			Min.	Typ.	Max.	单位
t_{ss}	软启动上升斜率	$R_{ADDR-TRISE}$=24kΩ 或 $R_{ADDR-TRISE}$≤20kΩ 或 MFR_SPEC_12[1:0]=00b	--	1	--	
		$R_{ADDR-TRISE}$=39kΩ 或 MFR_SPEC_12[1:0]=01b	--	1/2	--	
		$R_{ADDR-TRISE}$=75kΩ 或 MFR_SPEC_12[1:0]=10b	--	1/4	--	
		MFR_SPEC_12[1:0]=11b	--	1/8	--	

另外软启动时间还可以通过 MFR_SPECIFIC_07 进行调节：

MFR_SPECIFIC_07[2]SLEW_FAST:数据为 0 时，软启动上升斜率由 MFR_SPEC_13[2:0]设置；数据为 1 时：软启动上升斜率在 MFR_SPEC_13[2:0]设置的基础上增加 1.36mV/us。

MFR_SPECIFIC_07[0]SST_TIME:数据为 0 时，软启动上升斜率由 MFR_SPEC_12[1:0]设置；数据为 1 时：斜率改为 1/16。

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内部斜坡

KD12T-100A 模块的内部斜坡可通过 MFR_SPEC_14[2:0]设置，具体可参考下表：

斜坡设置			Min.	Typ.	Max.	单位
V_{RAMP}	斜坡设置	MFR_SPEC_14[2:0]=001b	30	40	50	mV_{P-P}
		MFR_SPEC_14[2:0]=011b	70	80	90	
		MFR_SPEC_14[2:0]=110b	135	145	155	
		MFR_SPEC_14[2:0]=111b	180	190	205	

模式设置

KD12T-100A 模块的 VR12 由 MFR_SPECIFIC_13 设置，具体可参考下表：

MODE 设置	
MFR_SPEC_13[7]	0:VR12.5 1:VR12.0

PMBus 地址位

KD12T-100A 模块的地址位可通过 ADDR_TRISE 引脚设置，具体可参考下表：

注：$R_{ADDR-TRISE}$ 还会影响到 VID 电压的设置以及软启动时间的设置，详情可查阅 **VID 数字调节输出电压**以及**软启动时间**。

地址位设置			
PADDR	PMBus 地址位设置 （$11P_4OP_2P_1P_0$）	$R_{ADDR-TRISE}$＜0.21kΩ	1100000
		0.62kΩ≤$R_{ADDR-TRISE}$≤0.78kΩ	1100001
		1.17kΩ≤$R_{ADDR-TRISE}$≤1.35kΩ	1100010
		1.80kΩ≤$R_{ADDR-TRISE}$≤2.00kΩ	1100011
		2.54kΩ≤$R_{ADDR-TRISE}$≤2.77kΩ	1100100
		3.41kΩ≤$R_{ADDR-TRISE}$≤3.69kΩ	1100101
		4.48kΩ≤$R_{ADDR-TRISE}$≤4.82kΩ	1100110
		5.79kΩ≤$R_{ADDR-TRISE}$≤6.21kΩ	1100111
		7.43kΩ≤$R_{ADDR-TRISE}$≤7.98kΩ	1110000
		9.56kΩ≤$R_{ADDR-TRISE}$≤10.31kΩ	1110001
		12.47kΩ≤$R_{ADDR-TRISE}$≤13.54kΩ	1110010
		16.58kΩ＜$R_{ADDR-TRISE}$≤18.24kΩ	1110011
		22.92kΩ≤$R_{ADDR-TRISE}$≤25.77kΩ	1110100
		33.96kΩ≤$R_{ADDR-TRISE}$≤39.77kΩ	1110101
		58.36kΩ≤$R_{ADDR-TRISE}$≤75.59kΩ	1110110

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NVM 默认设置

下表列出了所有 NVM 中的默认设置：

寄存器	功能	默认值							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MFR_SPECIFIC_13:[2:0]	Slew Rate						0	0	0
MFR_SPECIFIC_13:[7:3]	Mode	1	0	0	0	1			
MFR_SPECIFIC_09:[2:0]	OSR						1	1	1
MFR_SPECIFIC_09:[6:4]	USR		1	1	1				
MFR_SPECIFIC_11:[7:0]	VBOOT	1	0	0	1	0	1	1	1
MFR_SPECIFIC_12:[1:0]	TRISE							0	0
MFR_SPECIFIC_12:[7:4]	Frequency	0	0	0	0				
MFR_SPECIFIC_10:[7:0]	IMAX	1	1	1	0	1	0	0	1
MFR_SPECIFIC_00:[3:0]	OCL					1	1	1	1
MFR_SPECIFIC_14:[2:0]	RAMP								0
MFR_SPECIFIC_07:[0]	Soft-start slew rate								1
MFR_SPECIFIC_07:[1]	OSR_TRISTATE							1	
MFR_SPECIFIC_07:[2]	SLEW_FAST						0		
MFR_SPECIFIC_16:[1:0]	VIN_UVLO							0	0
MFR_SPECIFIC_15:[3]	DPS_TH_LOW					0			
MFR_SPECIFIC_15:[2:0]	DPS_TH_HIGH						0	0	1
MFR_SPECIFIC_22:[2:0]	UV OFFSET						0	1	1
MFR_SPECIFIC_05:[7:0]	VOUT OFFSET	0	0	0	0	0	0	0	0
MFR_ID	-	0	1	0	1	0	1	0	0
MFR_MODEL		0	1	0	0	0	1	1	1
MFR_REVISION:[3:0]						0	0	0	0
MFR_DATA		0	0	0	0	0	0	0	0

热设计

该产品可工作在不同的热环境下，但必须提供足够的散热以确保模块可靠运行。散热主要通过模块引脚到主板的热传导，以及流经模块的对流风速来实现。温度降额曲线提供了在特定 Vin 下的输出电流与环境温度和风速的关系。

该模块在 254 x 254 mm，8 层测试板上测试，并安装在截面为 608 x 203 mm 的风洞中。另外请注意模块和主板之间连接的低阻抗可有效减少额外的功率损耗。

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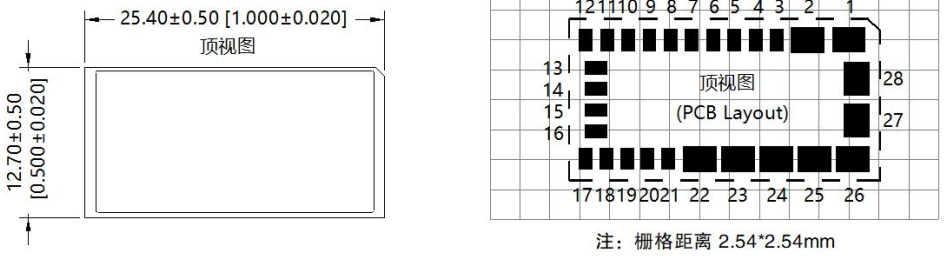
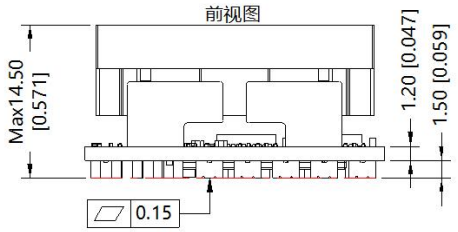
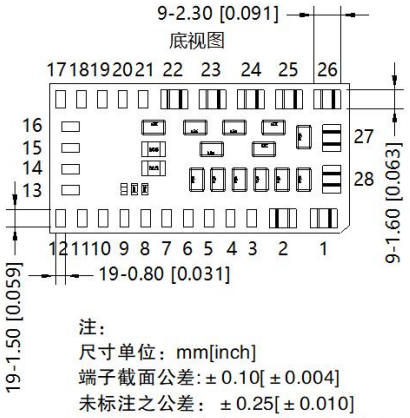
外观尺寸图

第三角投影



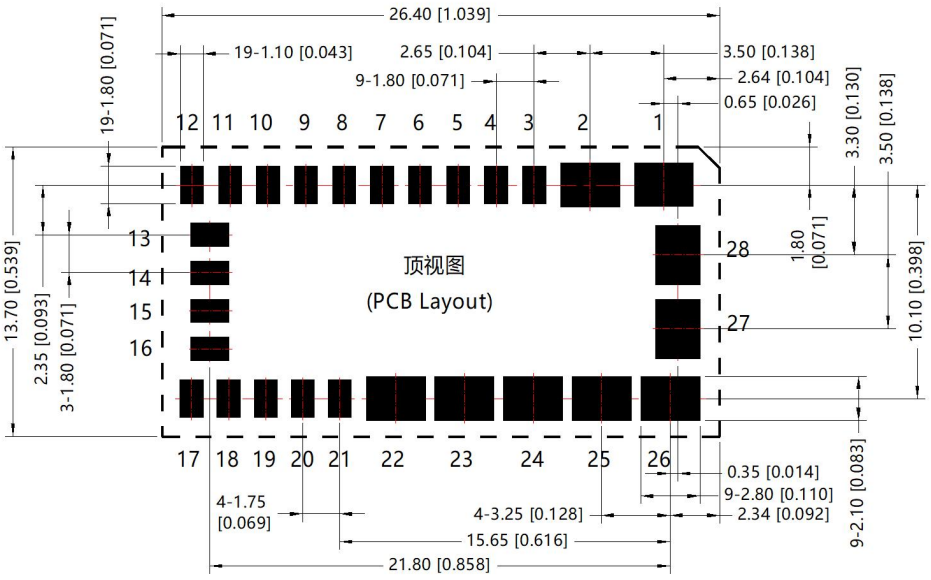
注：栅格距离 2.54*2.54mm





注：
尺寸单位：mm[inch]
端子截面公差:±0.10[±0.004]
未标注之公差：±0.25[±0.010]
器件布局仅供参考，具体以实物为准

引脚方式			
引脚	功能	引脚	功能
1	Vin	15	VREF
2	GND	16	NC
3	VR_RDY	17	VSP
4	V5	18	VSN
5	ENABLE	19	V3R3
6	TSEN	20	CSP3
7	PWM3	21	CSP4
8	PWM4	22	Vo
9	ADDR_TRISE	23	Vo
10	PMB_CLK	24	GND
11	PMB_DIO	25	Vo
12	PMB_ALERT#	26	Vo
13	AGND	27	GND
14	COMP	28	Vin



比例 2：1

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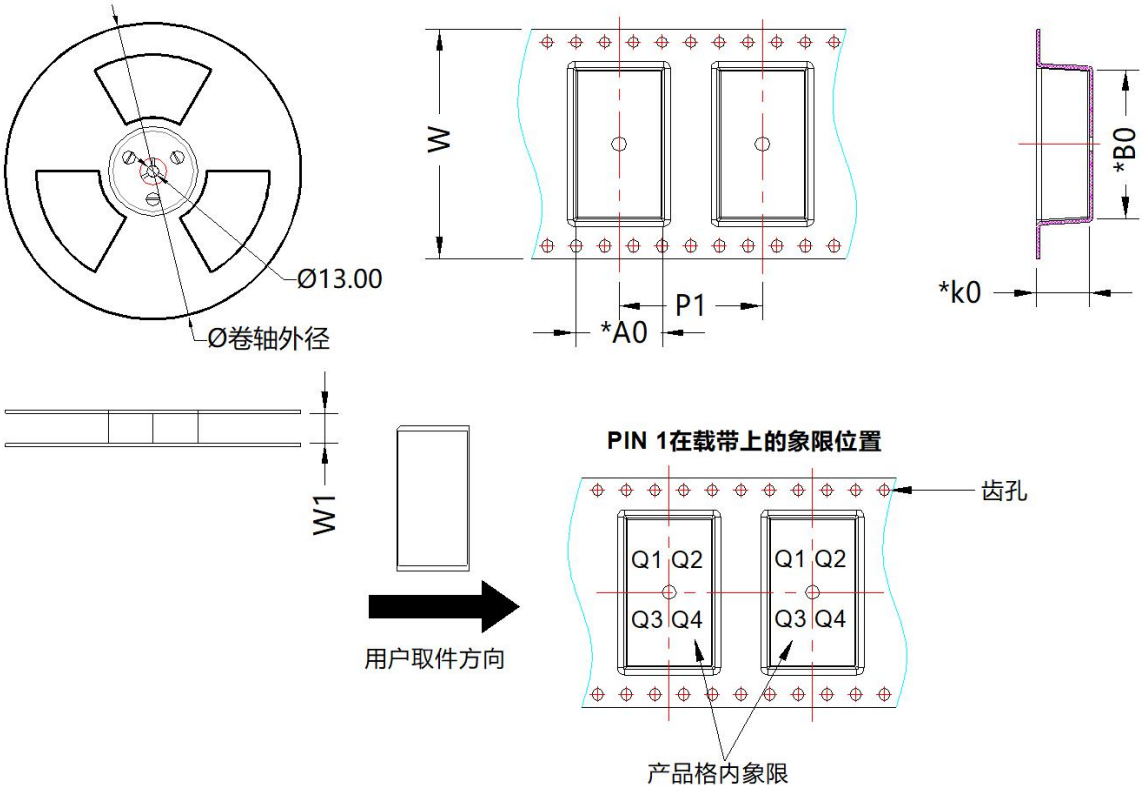
载带包装示意图



器件型号	封装类型	Pin	SPQ	卷轴外径 (mm)	卷轴宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限
KD12T-100A	SMD	28	160	330.0	44.4	14.08	26.58	14.26	24	44	Q1

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PMBus 描述

Commands Summary

CODE	COMMAND NAME	TYPE	DESCRIPTION	DEFAULT VALUE
01h	OPERATION	R/W Byte	Turn the unit on and off in conjunction with the input from the ENABLE pin. Set the output voltage to the upper or lower MARGIN voltages.	00h
02h	ON_OFF_CONFIG	R/W Byte	Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	17h
03h	CLEAR_FAULTS	Send Byte	Clears any faults bits that have been set if the fault is no longer present. At the same time, simultaneously clears all bits in all status registers and negates the PMB_ALERT signal output if it is asserted.	NONE
10h	WRITE_PROTECT	R/W Byte	Used to control writing to the PMBus device. Can be used to prevent unwanted writes to the device.	00h
11h	STORE_DEFAULT_ALL	Send Byte	Store the settings to the NVM.	NONE
12h	RESTORE_DEFAULT_ALL	Send Byte	Restore the settings from the NVM.	NONE
19h	CAPABILITY	Read Byte	Provides a way for the host to determine the capabilities of the PMBus device.	B0h
20h	VOUT_MODE	Read Byte	Read-Only VOUT Mode Indicator.	21h
21h	VOUT_COMMAND	R/W Word	Causes the device to set its output voltage to the commanded value.	VBOOT
24h	VOUT_MAX	R/W Word	Sets the upper limit on the output voltage the unit can command regardless of any other commands or combinations. Provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level.	00FFh
25h	VOUT_MARGIN_HIGH	R/W Word	Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High".	0000h
26h	VOUT_MARGIN_LOW	R/W Word	Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low."	0000h
39h	IOUT_CAL_OFFSET	R/W Word	compensate for offset errors in READ_VOUT command.	0000h
41h	VOUT_OV_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an output overvoltage fault.	80h
45h	VOUT_UV_FAULT_RESPONSE	Read Byte	Instructs fault. the device on what action to take in response to an output undervoltage	BAh
46h	IOUT_OC_FAULT_LIMIT	R/W Word	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition.	125% IMAX
47h	IOUT_OC_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an output overcurrent fault.	FAh
4Ah	IOUT_OC_WARN_LIMIT	R/W Word	Sets the value of the output current that causes an output overcurrent warning condition.	IMAX
4Fh	OT_FAULT_LIMIT	R/W Word	Sets the temperature, in degree Celsius, that causes an over-temperature fault condition.	007Dh

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50h	OT_FAULT_RESPONSE	Read Byte	Instructs fault. the device on what action to take in response to an output over-temperature	F8h
51h	OT_WARN_LIMIT	R/W Word	Sets the temperature, in degrees Celsius, that causes an over-temperature warning condition.	005Fh
55h	VIN_OV_FAULT_LIMIT	R/W Word	Sets the input voltage, in volts, that causes an overvoltage fault condition.	000Fh
5Bh	IIN_OC_FAULT_LIMIT	R/W Word	Sets the input current, in amperes, that causes an overcurrent fault condition.	00FFh
5Ch	IIN_OC_FAULT_RESPONSE	Read Byte	Instructs the device on what action to take in response to an input overcurrent fault.	C0h
5Dh	IIN_OC_WARN_LIMIT	R/W Word	Sets the input current, in amperes, that causes an overcurrent warning condition.	0019h
78h	STATUS_BYTE	Read Byte	Single byte status indicator	Dependent on the Startup Condition
79h	STATUS_WORD	Read Word	Full 2-byte status indicator	
7Ah	STATUS_VOUT	Read Byte	Output voltage fault status detail	
7Bh	STATUS_IOUT	Read Byte	Output current fault status detail	
7Ch	STATUS_INPUT	Read Byte	Input voltage and current fault status detail	
7Dh	STATUS_TEMPERATURE	Read Byte	Temperature fault status detail	
7Eh	STATUS_CML	Read Byte	Communication, memory, and logic fault status detail	
80h	STATUS_MFR_SPECIFIC	Read Byte	Manufacturer specific fault status detail	
88h	READ_VIN	Read Word	Read input voltage, in volts.	
89h	READ_IIN	Read Word	Read input current, in amperes.	
8Bh	READ_VOUT	Read Word	Read output voltage, in volts.	
8Ch	READ_IOUT	Read Word	Read output current, in amperes.	
8Dh	READ_TEMPERATURE_1	Read Word	Read temperature, in degrees Celsius.	
96h	READ_POUT	Read Word	Read output power, in watts.	
97h	READ_PIN	Read Word	Read input power, in watts.	
98h	PMBUS_REVISION	Read Byte	PMBus Revision Information	11h
99h	MFR_ID	Read Block	Loads the unit with the text character that contains the manufacturer's ID.	5401h
9Ah	MFR_MODEL	Read Block	Loads the unit with the text character that contains the model number of the manufacturer.	4701h
9Bh	MFR_REVISION	Read Block	Loads the unit with the text character that contains the revision number of the manufacturer.	
9Dh	MFR_DATE	Read Block	Loads the unit with the text character that contains the device's date of manufacture.	
A4h	MFR_VOUT_MIN	R/W Word	Sets a low limit on the output voltage that the device can command regardless of any other commands or combinations. (VID data format)	000h
D0h	MFR_SPECIFIC_00	R/W Byte	Selects the threshold for the per-phase current limit. (Fixed at PMBus control)	0Fh
D1h	MFR_SPECIFIC_01	R/W Byte	Selects the averaging time for telemetry reporting.	50h
D4h	MFR_SPECIFIC_04	Read Word	Returns the actual, measured output voltage in volts.	
D5h	MFR_SPECIFIC_05	R/W Byte	Used to trim the output voltage.	00h

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D7h	MFR_SPECIFIC_07	R/W Byte	Additional functional bits setting.	03h
D8h	MFR_SPECIFIC_08	R/W Byte	Sets the droop as a percentage of the loadline.	04h
D9h	MFR_SPECIFIC_09	R/W Byte	Sets the threshold for OSR and USR control.	77h
DAh	MFR_SPECIFIC_10	R/W Byte	Sets the maximum operating current, IMAX.	E9h
DBh	MFR_SPECIFIC_11	R/W Byte	Sets the boot voltage, VBOOT.	97h
DCh	MFR_SPECIFIC_12	R/W Byte	Sets the switching frequency and the rise time (tRISE) settings.	00h
DDh	MFR_SPECIFIC_13	R/W Byte	Sets the slew rate and other operation modes.	88h
DEh	MFR_SPECIFIC_14	R/W Byte	Sets the ramp amplitude in mV.	06h
DFh	MFR_SPECIFIC_15	R/W Byte	Sets the threshold for dynamic phase shedding as a percentage of the OCL.	01h
E0h	MFR_SPECIFIC_16	R/W Byte	Sets the threshold for the input voltage UVLO.	00h
E4h	MFR_SPECIFIC_20	R/W Byte	Sets the maximum number of operational phase numbers on the fly.	Hardware Specific
FCh	MFR_SPECIFIC_44	Read Word	Returns DEVICE_CODE information	01F0h

PMBus General

Timing and electrical characteristics of the PMBus can be found in the PMB Power Management Protocol Specification, Part 1, revision 1.1 available at http://PMBus.org. The KD12T-100A device supports both the 100-kHz and 400-kHz bus timing requirements. The KD12T-100A device does not stretch pulses on the PMBus when communicating with the master device.

Communication over the KD12T-100A device PMBus interface can support the packet error checking (PEC) scheme if desired. If the master supplies CLK pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The KD12T-100A device supports a subset of the commands in the PMBus 1.1 specification. Most of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the KD12T-100A device. See the Supported PMBus Commands section for specific details.

The KD12T-100A device also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the KD12T-100A device) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The KD12T-100A device contains non-volatile memory that is used to store configuration settings and scale factors. The settings programmed into the device are not automatically saved into this non-volatile memory though. The STORE_DEFAULT_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

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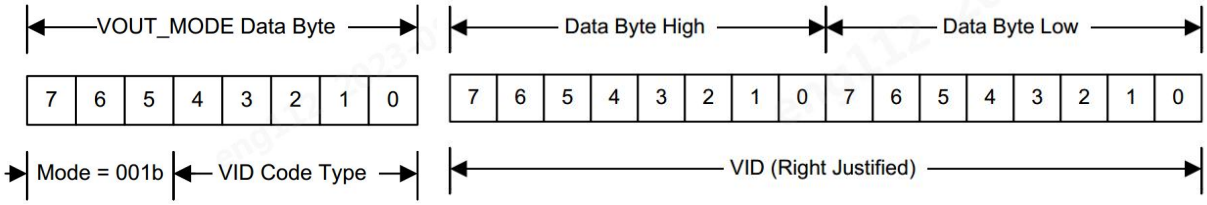
PMBus Connections

The KD12T-100A device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s). Connection for the PMBus interface should follow the High Power DC specifications given in Section 3.1.3 of the System Management Bus (SMBus) Specification V2.0 for the 400-kHz bus speed or the Low Power DC specifications in Section 3.1.2. The complete SMBus specification is available from the SMBus website, smbus.org.

Supported Data Formats

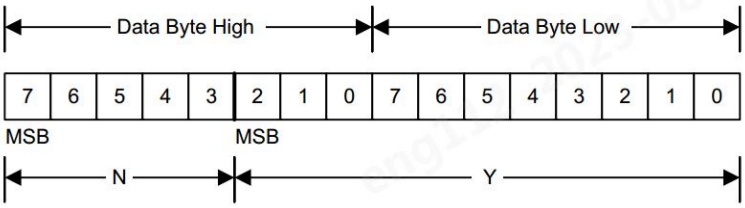
The KD12T-100A device supports both linear and VID data formats. The linear data format is used for all telemetry reporting data, and VID formatting for certain other commands. (see the Supported PMBus Commands section for more details on which command supports each data type). Examples of commands that support VID formatting include VOUT_MODE (Read-only Byte) and VOUT_COMMAND (Read/Write Word). An example of each can be seen in below Figure.



The Linear Data Format is a two byte value with:

- An 11-bit, two's complement mantissa, and
- A 5-bit, two's complement exponent (scaling factor).

The format of the two bytes is shown in below Figure.



The relation between Y, N, and the real world value is as shown in below Equation.

$$X = Y \times 2^{N}$$

where

- X is the real world value
- Y is an 11-bit, two's complement integer
- N is a 5-bit, two's complement integer

Note that devices that use the Linear format must accept and be able to process any value of N.

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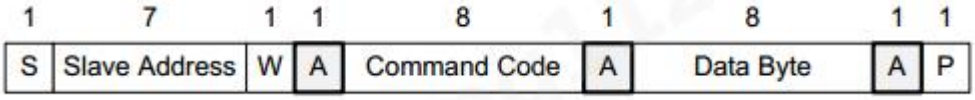
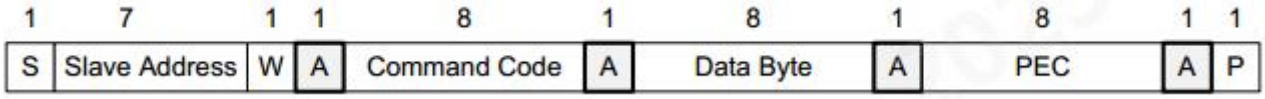
PMBus Command Format

The KD12T-100A device is a PMBus-compliant device. Below Figure show the major communication protocols used. For full details on the PMBus communication protocols, please visit http://pmbus.org.



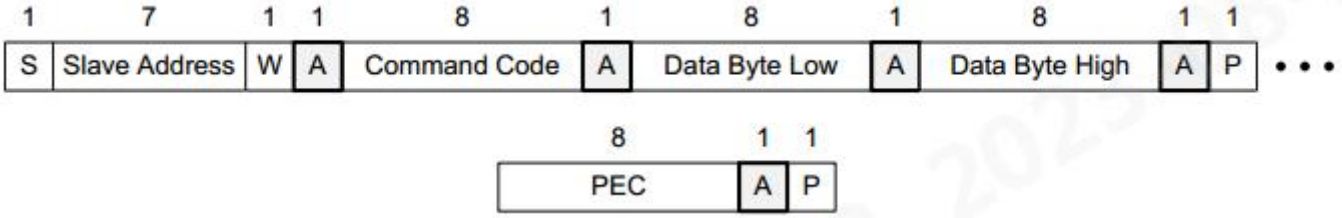
Write Byte Protocol



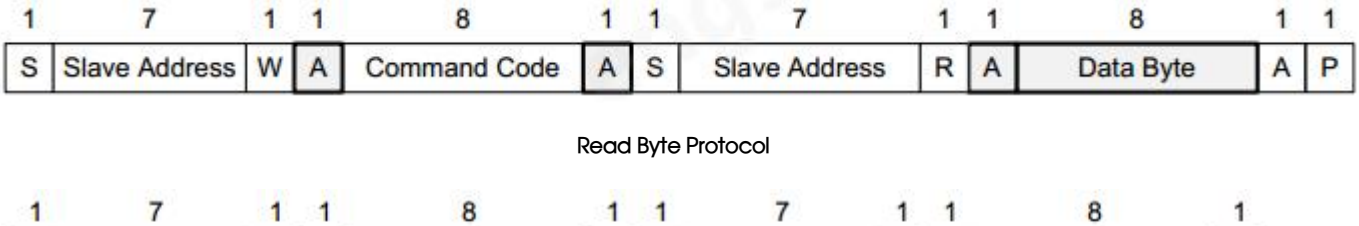
Write Byte Protocol with PEC



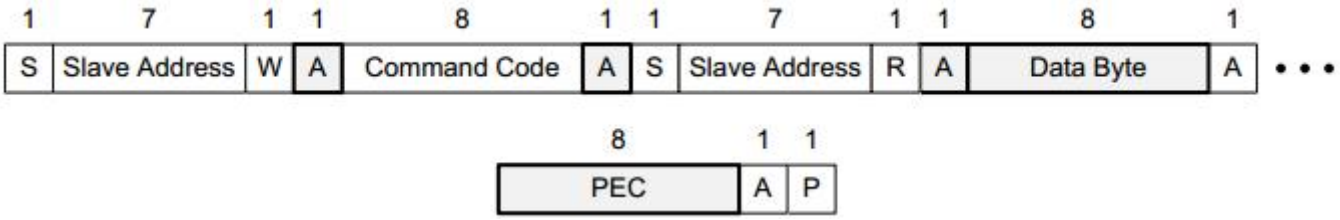
Write Word Protocol



Write Word Protocol with PEC



Read Byte Protocol



Read Byte Protocol with PEC

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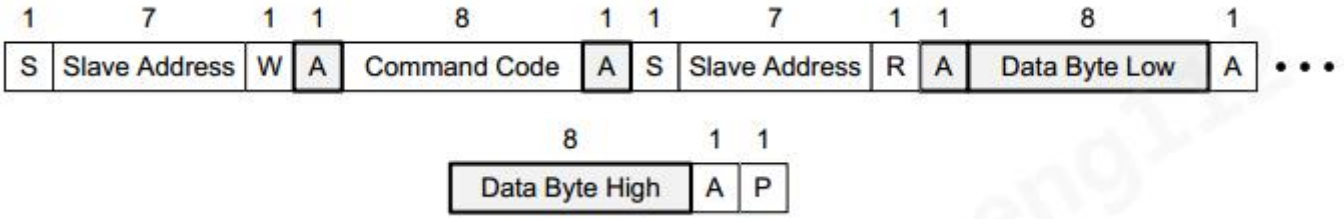
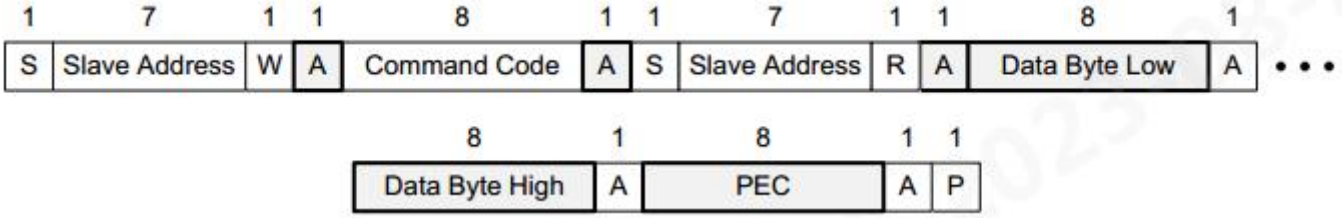
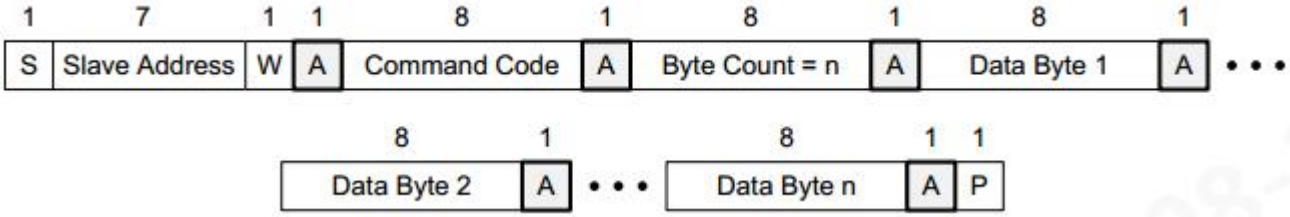


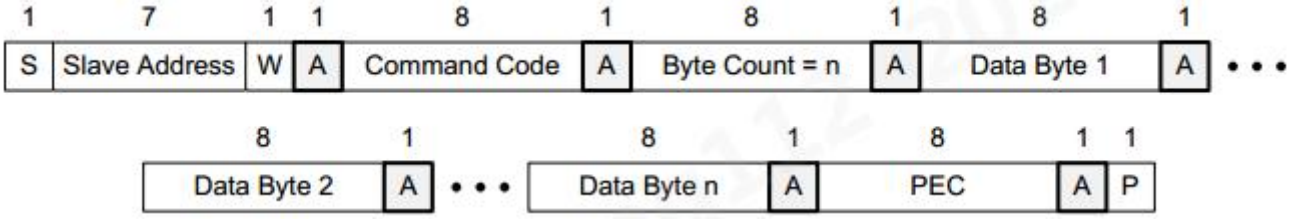
Read Word Protocol



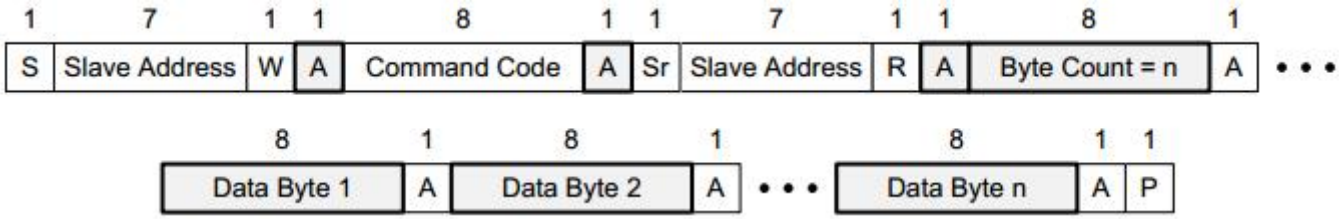
Read Word Protocol with PEC



Block Write Protocol



Block Write Protocol with PEC



Block Read Protocol



Block Read Protocol with PEC

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PMBus 寄存器

OPERATION (01h)

Format	N/A
Description	The OPERATION command is used to turn the device output on or off in conjunction with the input from the ENABLE pin. It is also used to set the output voltage to the upper or lower MARGIN levels.
Default	00h

7	6	5	4	3	2	1	0
ON_OFF	SOFT_OFF	OPMARGIN				IIN_OC_VRHOT	
R/W	R-0	R/W				R/W	

Bits	Field	Type	Reset	NVM	Description
7	ON_OFF	R/W	0	--	The On/Off bit is used to enable the IC via PMBus. The necessary condition for this bit to be effective is that the CMD bit in the ON_OFF CONFIG register is set high. However, the CMD bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit CP in the ON_OFF CONFIG register is low, or c. The bit CP is high and the ENABLE pin is asserted.
6	SOFT_OFF	R	0	--	This bit is not supported and always set to 0 on this device. 0: No Soft off 1: Not Supported.
5:2	OPMARGIN	R/W	0	--	If Margin Low is enabled, load the value from the VOUT_MARGIN_LOW register. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH register. 00xx: Turn off VOUT margin function 0101: Turn on VOUT margin low and ignore fault 0110: Turn on VOUT margin low and act on fault 1001: Turn on VOUT margin high and ignore fault 1010: Turn on VOUT margin high and act on fault
1:0	IIN_OC_VRHOT	R/W	00	--	This bit sets the option of asserting VRHOT when IIN_OC_WARN_LIMIT is detected. 01: VRHOT assertion ON with IIN_OC_WARN_LIMIT detection others: VRHOT assertion OFF with IIN_OC_WARN_LIMIT detection

ON_OFF_CONFIG (02h)

Format	N/A
Description	The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.
Default	17h

7	6	5	4	3	2	1	0
Reserved			PU	CMD	CP	PL	SP
R-000			R-1	R/W	R/W	R-1	R-1

Bits	Field	Type	Reset	NVM	Description
7:5	RESERVED	R	000	--	Always set to 0.
4	PU	R	1	--	This bit is not supported and always set to 1 on this device. 0: Not supported. 1: Device will act on ENABLE pin assertion and/or ON_OFF bit (OPERATION<7>).
3	CMD	R/W	0	--	The CMD bit controls how the device responds to the OPERATION<7> bit. 0: (Default) Device ignores the ON_OFF OPERATION<7> bit. 1: Device responds to the ON_OFF OPERATION<7> bit.
2	CP	R/W	1	--	The CP bit controls how the device responds to the ENABLE pin 0: Device ignores the ENABLE pin, and ON/OFF is controlled only by the OPERATION command 1: Device responds to the ENABLE pin.

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1	PL	R	1	--	This bit is not supported and always set to 1 on this device. 0: Not supported. 1: ENABLE pin has active high polarity.
0	SP	R	1	--	This bit is not supported and always set to 1 on this device. 0: Not supported. 1: Turn off output as fast as possible.

CLEAR_FAULTS (03h)

Format	N/A
Description	Clears any faults bits that have been set. At the same time, simultaneously clears all bits in all status registers and negates the PMB_ALERT signal output if it is asserted. The CLEAR_FAULTS command does not cause a unit that has latched off for a condition to restart. If the fault remains present when the bit is cleared, the fault bit is reset and the host notified by the usual means.
Default	NONE

7	6	5	4	3	2	1	0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
--	--	--	--	--	--	--	--

Bits	Field	Type	Reset	NVM	Description
7:0	N/A	--	--	--	No data bytes are sent, only the command code is sent.

WRITE_PROTECT (10h)

Format	N/A
Description	The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command has one data byte as described below. NOTE: Invalid data written to WRITE_PROTECT(7:5) causes the ‘CML’ bit in the STATUS_BYTE and the ‘US_DATA’ bit in the STATUS_CML registers to be set. Invalid data also results in no write protection.
Default	NONE

7	6	5	4	3	2	1	0
Bit7	Bit6	Bit5	Reserved				
R/W	R/W	R/W	R-0 0000				

Bits	Field	Type	Reset	NVM	Description
7	Bit7	R/W	0	--	0: (Default) See Table 12. 1: Disable all writes except for the WRITE_PROTECT command (bit5 and bit6 must be 0 to be valid).
6	Bit6	R/W	0	--	0: (Default) See Table 12. 1: Disable all writes except for the WRITE_PROTECT and OPERATION commands (bit5 and bit7 must be 0 to be valid).
5	Bit5	R/W	0	--	0: (Default) See Table 12. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and ON_OFF_CONFIG commands (bit6 and bit7 must be 0 to be valid).
4:0	Reserved	R	00000	--	Always set to 0.

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Data Byte Value	Action
1000 0000	Disables all writes except to the WRITE_PROTECT command.
0100 0000	Disables all writes except to the WRITE_PROTECT and OPERATION commands.
0010 0000	Disables all writes to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND commands.
0000 0000	Enable writes to all commands
Others	Invalid data.

STORE_DEFAULT_ALL (11h)

Format	N/A
Description	The STORE_DEFAULT_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the nonvolatile Default Store memory. Any items in the Operating Memory that do not have matching locations in the Default Store are ignored. Following a STORE_DEFAULT_ALL command, the following registers return to the default values regardless of the values in the Operating Memory: • OC_FAULT_LIMIT returns to 125%xIMAX, • OC_WARN_LIMIT returns to IMAX, • VOUT_COMMAND returns to VBOOT, • VOUT_MAX returns to 00FFh (1.52V in VR12.0 mode and 3.04 V in VR12.5 mode)
Default	NONE

7	6	5	4	3	2	1	0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
--	--	--	--	--	--	--	--

Bits	Field	Type	Reset	NVM	Description
7:0	N/A	--	--	--	No data bytes are sent, only the command code is sent.

RESTORE_DEFAULT_ALL (12h)

Format	N/A
Description	The RESTORE_DEFAULT_ALL command instructs the PMBus device to copy the entire contents of the non-volatile Default Store memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the Default Store. Any items in Default Store that do not have matching locations in the Operating Memory are ignored.
Default	NONE

7	6	5	4	3	2	1	0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
--	--	--	--	--	--	--	--

Bits	Field	Type	Reset	NVM	Description
7:0	N/A	--	--	--	No data bytes are sent, only the command code is sent.

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CAPABILITY (19h)

Format	N/A
Description	This command provides a way for a host system to determine some key capabilities of this PMBus device.
Default	B0h

7	6	5	4	3	2	1	0
PEC	SPD		PMBALERT	Reserved			
R-1	R-01		R-1	R-0000			

Bits	Field	Type	Reset	NVM	Description
7	PEC	R	1	--	Packet Error Checking is supported. 1: Default
6:5	SPD	R	01	--	Maximum supported bus speed is 400 kHz. 01: Default
4	PMBALERT	R	1	--	This device does have a PMBALERT pin and does support the SMBus Alert Response Protocol. 1: Default
3:0	Reserved	R	0000	--	Always set to 0.

VOUT_MODE (20h)

Format	VID
Description	The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below. This command is read-only. If the host sends a VOUT_MODE command for writing, the device will reject the command and declare a communication fault for invalid data and respond as described in PMBus specification II section 10.2.2.
Default	21h

7	6	5	4	3	2	1	0
DATA_MODE			DATA_PARAMETER				
R-001			R-0 0001				

Bits	Field	Type	Reset	NVM	Description
7:5	DATA_MODE	R	001	--	001: VID mode.
4:0	DATA_PARAMETER	R	0 0001	--	00010: For VR12.5 Mode 00001: For VR12.0 Mode

VOUT_COMMAND (21h)

Format	VID
Description	VOUT_COMMAND causes the device to set its output voltage to the commanded value with two data bytes. These data bytes consist of a right-justified VID code with VID0 in bit 0 of the lower data byte, VID1 in bit 1 of the lower byte and so forth. The VID table mapping is determined by the selected VID protocols (VR12.0 or VR12.5) from SLEW_MODE pin or MFR_SPECIFIC_13.
Default	VBOOT

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							

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7	6	5	4	3	2	1	0
VOUT							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:8	Reserved	R	0000 0000	--	Always set to 0.
7:0	VOUT	R/W	VBOOT	--	Used to set the commanded VOUT. Cannot be set to a level above the value set by VOUT_MAX.

VOUT_MAX (24h)

Format	VID
Description	The VOUT_MAX command sets an upper limit on the output voltage that the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. The device detects that an attempt has been made to program the output to a voltage greater than the value set by the VOUT_MAX command. This will then be treated as a warning condition and not a fault condition. If an attempt is made to program the output voltage higher than the limit set by this command, the device responds as follows: • The commanded output voltage is set to VOUT_MAX, • The OTHER bit is set in the STATUS_BYTE, • The VOUT bit is set in the STATUS_WORD, • The VOUT_MAX warning bit is set in the STATUS_VOUT register, and • The device notifies the host (asserts PMBUS_ALERT). The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols (VR12.0 or VR12.5) from the SLEW_MODE pin or MFR_SPECIFIC_13.
Default	00FFh

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							

7	6	5	4	3	2	1	0
VOUT_MAX							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:8	Reserved	R	0000 0000	--	Always set to 0.
7:0	VOUT_MAX	R/W	1111 1111	--	Used to set the maximum VOUT of the device.

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VOUT_MARGIN_HIGH (25h)

Format	VID
Description	The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to Margin High. The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.
Default	0000h

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							

7	6	5	4	3	2	1	0
VOUT_MARGIN_HIGH							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:8	Reserved	R	0000 0000	--	Always set to 0.
7:0	VOUT_MARGIN_HIGH	R/W	0000 0000	--	Used to set the value for the VOUT Margin High.

VOUT_MARGIN_LOW (26h)

Format	VID
Description	The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to Margin Low. The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.
Default	0000h

15	14	13	12	11	10	9	8
Reserved							
R-0000 0000							

7	6	5	4	3	2	1	0
VOUT_MARGIN_LOW							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:8	Reserved	R	0000 0000	--	Always set to 0.
7:0	VOUT_MARGIN_LOW	R/W	0000 0000	--	Used to set the value for the VOUT Margin Low.

IOUT_CAL_OFFSET (39h)

Format	Linear
Description	The IOUT_CAL_OFFSET command sets the value of compensation for offset errors in the READ_IOUT command, in amperes.
Default	0000h

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15	14	13	12	11	10	9	8
IOCAL_OFS_EXPONENT					IOCAL_OFS_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
IOCAL_OFS_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	IOCAL_OFS_EXPONENT	R/W	--	--	5-bit, two's complement exponent (scaling factor).
10:0	IOCAL_OFS_MANTISSA	R/W	--	--	5-bit, two's complement exponent (scaling factor).

VOUT_OV_FAULT_RESPONSE (41h)

Format	N/A
Description	The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. Upon triggering the overvoltage fault, the controller is latched off, and the following actions are taken: • Set the VOUT_OV_FAULT bit in the STATUS_BYTE, • Set the VOUT bit in the STATUS_WORD, • Set the VOUT_OV_FAULT bit in the STATUS_VOUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	80h

7	6	5	4	3	2	1	0
VOUT_OV_FAULT_RESPONSE							
R-1000 0000							

Bits	Field	Type	Reset	NVM	Description
7:0	VOUT_OV_FAULT_RESPONSE	R	1000 0000	--	Upon triggering the overvoltage fault, the controller will shut the device down immediately and will not attempt to restart. The output remains disabled until the fault is cleared.

VOUT_UV_FAULT_RESPONSE (45h)

Format	N/A
Description	The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault. Upon triggering the undervotlage fault, the following actions are taken: • Set the OTHER bit in the STATUS_BYTE, • Set the VOUT bit in the STATUS_WORD, • Set the VOUT_UV_FAULT bit in the STATUS_VOUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	BAh

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7	6	5	4	3	2	1	0
VOUT_UV_FAULT_RESPONSE							
R-1011 1010							

Bits	Field	Type	Reset	NVM	Description
7:0	VOUT_UV_FAULT_RESPONSE	R	1011 1010	--	Upon triggering the undervoltage fault, the controller will shut the device down immediately and will attempt to restart after a 22 ms delay.

IOUT_OC_FAULT_LIMIT (46h)

Format	Linear
Description	The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes an overcurrent fault condition. Upon triggering the overcurrent fault, the following actions are taken: • Set the IOUT_OC_FAULT bit in the STATUS_BYTE, • Set the IOUT bit in the STATUS_WORD, • Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and • The device notifies the host (asserts PMB_ALERT)
Default	125% IMAX

15	14	13	12	11	10	9	8
OCF_LIMIT_EXPONENT					OCF_LIMIT_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
OCF_LIMIT_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	OCF_LIMIT_EXPONENT	R/W	--	--	5-bit, two's complement exponent (scaling factor).
10:0	OCF_LIMIT_MANTISSA	R/W	--	--	11-bit, two's complement mantissa.

IOUT_OC_FAULT_LIMIT (47h)

Format	N/A
Description	The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to an output overcurrent fault. Upon triggering the overcurrent fault, the controller is latched off, and the following actions are taken: • Set the IOUT_OC_FAULT bit in the STATUS_BYTE, • Set the IOUT bit in the STATUS_WORD, • Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	FAh

7	6	5	4	3	2	1	0
IOUT_OC_FAULT_RESPONSE							
R-1111 1010							

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Bits	Field	Type	Reset	NVM	Description
7:0	IOUT_OC_FAULT_RESPONSE	R	1111 1010	--	Upon triggering the overcurrent fault, the controller immediately shuts down the device and attempts to restart after a 22 ms delay.

IOUT_OC_WARN_LIMIT (4Ah)

Format	Linear
Description	The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes an output overcurrent warning condition. Upon triggering the overcurrent warning, the following actions are taken: • Set the OTHER bit in the STATUS_BYTE, • Set the IOUT bit in the STATUS_WORD, • Set the IOUT OC Warning bit in the STATUS_IOUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	IMAX

15	14	13	12	11	10	9	8
OCW_LIMIT_EXPONENT					OCW_LIMIT_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
OCW_LIMIT_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	OCW_LIMIT_EXPONENT	R/W	--	--	5-bit, two's complement exponent (scaling factor).
10:0	OCW_LIMIT_MANTISSA	R/W	--	--	11-bit, two's complement mantissa.

OT_FAULT_LIMIT (4Fh)

Format	Linear
Description	The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition. The default value is 125C°. Upon triggering the over-temperature fault, the following actions are taken: • Set the TEMPERATURE bit in the STATUS_BYTE, • Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and • The device notifies the host (asserts PMB_ALERT and VR_FAULT).
Default	007Dh

15	14	13	12	11	10	9	8
OT_LIMIT_EXPONENT					OT_LIMIT_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
OT_LIMIT_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	OT_LIMIT_EXPONENT	R/W	0000 0	--	5-bit, two's complement exponent (scaling factor).
10:0	OT_LIMIT_MANTISSA	R/W	000 0111 1101	--	11-bit, two's complement mantissa.

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OT_FAULT_RESPONSE (50h)

Format	N/A
Description	The OT_FAULT_RESPONSE instructs the device on what action to take in response to an over-temperature fault. Upon triggering the over-temperature fault, the controller shuts off and attempts to restart when the temperature reduces by 15C°, and the following actions are taken: • Set the TEMPERATURE bit in the STATUS_BYTE, • Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and • The device notifies the host (asserts PMB_ALERT and VR_FAULT).
Default	F8h

7	6	5	4	3	2	1	0
OT_FAULT_RESPONSE							
R-1111 1000							

Bits	Field	Type	Reset	NVM	Description
7:0	OT_FAULT_RESPONSE	R	1111 1000	--	Upon triggering the over-temperature fault, the device will shut down immediately (disables the output), and will restart when the temperature goes 15 degree Celsius below OT _FAULT_LIMIT.

OT_WARN_LIMIT (51h)

Format	Linear
Description	The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, at which it should indicate an over-temperature warning condition. The default value is 95C. Upon triggering the over-temperature warning, the following actions are taken: • Sets the TEMPERATURE bit in the STATUS_BYTE, • Sets the OT Warning bit in the STATUS_TEMPERATURE register, and • The device notifies the host (asserts PMB_ALERT).
Default	005Fh

15	14	13	12	11	10	9	8
OTW_WARN_EXPONENT					OTW_WARN_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
OTW_WARN_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	OTW_WARN_EXPONENT	R/W	0000 0	--	5-bit, two's complement exponent (scaling factor).
10:0	OTW_WARN_MANTISSA	R/W	000 0101 1111	--	11-bit, two's complement mantissa.

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VIN_OV_FAULT_LIMIT (55h)

Format	Linear
Description	The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an input overvoltage fault condition. The default value is 17 V in NVM mode and 14 V in pinstrap mode. Upon triggering an input voltage fault, the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the upper byte of the STATUS_WORD, • Sets the VIN_OV_FAULT bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	000Fh

15	14	13	12	11	10	9	8
VIN_OVF_EXPONENT					VIN_OVF_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
VIN_OVF_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	VIN_OVF_EXPONENT	R/W	0000 0	--	5-bit, two's complement exponent (scaling factor).
10:0	VIN_OVF_MANTISSA	R/W	000 0001 0001	--	11-bit, two's complement mantissa.

After a STORE_DEFAULT_ALL command, the controller reads the last two LSB of VIN_OV_FAULT_LIMIT and convert to decimal, and then adds 14 and converts to save into the VIN_OV_FAULT_LIMIT register. For example, when the two LSB are 01b, after STORE_DEFAULT_ALL command, the VIN_OV_FAULT_LIMIT reads 000Fh (15 V).

IIN_OC_FAULT_LIMIT (5Bh)

Format	Linear
Description	The IIN_OC_FAULT_LIMIT command sets the value of the input current, in amperes, that the causes an input overcurrent fault condition. Upon triggering the overcurrent fault, the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the STATUS_WORD, • Sets the IIN_OC_FAULT bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	00FFh

15	14	13	12	11	10	9	8
INOCF_LIMIT_EXPONENT					INOCF_LIMIT_MANTISSA		
R/W					R/W		

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7	6	5	4	3	2	1	0
INOCF_LIMIT_MANTISSA							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:11	INOCF_LIMIT_EXPONENT	R/W	0000 0	--	5-bit, two's complement exponent (scaling factor).
10:0	INOCF_LIMIT_MANTISSA	R/W	000 1111 1111	--	11-bit, two's complement mantissa.

IIN_OC_FAULT_RESPONSE (5Ch)

Format	N/A
Description	The IIN_OC_FAULT_RESPONSE instructs the device on what action to take in response to an input overcurrent fault. Upon triggering the input overcurrent fault, the controller is latched off, and the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the STATUS_WORD, • Sets the IIN_OC_FAULT bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT and VR_FAULT).
Default	C0h

7	6	5	4	3	2	1	0
IIN_OC_FAULT_RESPONSE							
R-1100 0000							

Bits	Field	Type	Reset	NVM	Description
7:0	IIN_OC_FAULT_RESPONSE	R	1100 0000	--	Upon triggering the input overcurrent fault, the device will shut down immediately (disables the output), and will not attempt to restart. The output then remains disabled until the fault is cleared.

IIN_OC_WARN_LIMIT (5Dh)

Format	Linear
Description	The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes the input overcurrent warning condition. The default setting is 25A. Upon triggering the overcurrent warning, the following actions are taken: • Sets the OTHER bit in the STATUS_BYTE, • Sets the INPUT bit in the STATUS_WORD, • Sets the IIN OC Warning bit in the STATUS_INPUT register, and • The device notifies the host (asserts PMB_ALERT).
Default	0019h

15	14	13	12	11	10	9	8
INOCW_LIMIT_EXPONENT					INOCW_LIMIT_MANTISSA		
R/W					R/W		

7	6	5	4	3	2	1	0
INOCW_LIMIT_MANTISSA							
R/W							

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Bits	Field	Type	Reset	NVM	Description
15:11	INOCW_LIMIT_EXPONENT	R/W	0000 0	--	5-bit, two's complement exponent (scaling factor).
10:0	INOCW_LIMIT_MANTISSA	R/W	000 0001 1001	--	11-bit, two's complement mantissa.

STATUS_BYTE (78h)

Format	N/A
Description	The STATUS_BYTE command returns a single byte of information with the a summary of critical faults. The STATUS_BYTE command is the same register as the low byte of the STATUS_WORD command. It should be noted that all faults and warnings trigger the assertion of PMB_ALERT.
Default	00h

7	6	5	4	3	2	1	0
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER
R-0	R	R	R	R	R	R	R

Bits	Field	Type	Reset	NVM	Description
7	BUSY	R	0	--	Not supported and always set to 0
6	OFF	R	--	--	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	--	--	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	--	--	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	--	--	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	--	--	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	--	--	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	--		Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits (6:1) in this register. 0: No fault has occurred 1: A fault or warning not listed in bits (6:1) has occurred.

STATUS_WORD (79h)

Format	N/A
Description	The STATUS_WORD command returns two bytes of information with a summary of critical faults, such as over-voltage, overcurrent, over-temperature, etc. It should be noted that all faults and warnings except VIN_UV trigger the assertion of PMB_ALERT. NOTE: The STATUS_WORD low byte is the STATUS_BYTE.
Default	0000h

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15	14	13	12	11	10	9	8
VOUT	IOUT	INPUT	MFR	PGOOD	FANS	OTHER	UNKNOWN
R	R	R	R	R	R-0	R-0	R-0

7	6	5	4	3	2	1	0
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER
R-0	R	R	R	R	R	R	R

Bits	Field	Type	Reset	NVM	Description
15	VOUT	R	--	--	Output Voltage Fault/Warning 0: Latched flag indicating no VOUT fault or warning has occurred. 1: Latched flag indicating a VOUT fault or warning has occurred.
14	IOUT	R	--	--	Output Current Fault/Warning 0: Latched flag indicating no IOUT fault or warning has occurred. 1: Latched flag indicating an IOUT fault or warning has occurred.
13	INPUT	R	--	--	Input Voltage/Current Fault/Warning 0: Latched flag indicating no VIN or IIN fault or warning has occurred. 1: Latched flag indicating a VIN or IIN fault or warning has occurred.
12	MFR	R	--	--	MFR_SPECIFIC Fault 0: Latched flag indicating no MFR_SPECIFIC fault has occurred. 1: Latched flag indicating a MFR_SPECIFIC fault has occurred.
11	PGOOD	R	--	--	Power Good Status 0: Raw status indicating VRRDY pin is at logic high. 1: Raw status indicating VRRDY pin is at logic low.
10	FANS	R	0	--	Not supported and always set to 0.
9	OTHER	R	0	--	Not supported and always set to 0.
8	UNKNOWN	R	0	--	Not supported and always set to 0.
7	BUSY	R	0	--	Not supported and always set to 0
6	OFF	R	--	--	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	--	--	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	--	--	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	--	--	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	--	--	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	--	--	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	--	--	Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits (6:1) in this register. 0: No fault has occurred 1: A fault or warning not listed in bits (6:1) has occurred.

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STATUS_VOUT (7Ah)

Format	N/A
Description	The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.
Default	00h

7	6	5	4	3	2	1	0
VOUT_OVF	VOUT_OVW	VOUT_UVW	VOUT_UVF	VOUT_MAXW	TON_MAX	TOFF_MAX	VOUT_TRACK
R	R-0	R-0	R	R	R-0	R-0	R-0

Bits	Field	Type	Reset	NVM	Description
7	VOUT_OVF	R	--	--	Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred.
6	VOUT_OVW	R	0	--	Not supported and always set to 0.
5	VOUT_UVW	R	0	--	Not supported and always set to 0.
4	VOUT_UVF	R	--	--	Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred.
3	VOUT_MAXW	R	--	--	VOUT Max Warning 0: Latched flag indicating that no VOUT Max warning has occurred 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
2	TON_MAX	R	0	--	Not supported and always set to 0.
1	TOFF_MAX	R	0	--	Not supported and always set to 0.
0	VOUT_TRACK	R	0	--	Not supported and always set to 0.

STATUS_IOUT (7Bh)

Format	N/A
Description	The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.
Default	00h

7	6	5	4	3	2	1	0
IOUT_OCF	IOUT_OCUVF	IOUT_OCW	IOUT_UCF	CUR_SHAREF	POW_LIMIT	POUT_OPF	POUT_OPW
R	R-0	R	R-0	R-0	R-0	R-0	R-0

Bits	Field	Type	Reset	NVM	Description
7	IOUT_OCF	R	--	--	Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred.
6	IOUT_OCUVF	R	0	--	Not supported and always set to 0.
5	IOUT_OCW	R	0	--	Not supported and always set to 0.
4	IOUT_UCF	R	--	--	Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred.
3	CUR_SHAREF	R	--	--	VOUT Max Warning 0: Latched flag indicating that no VOUT Max warning has occurred 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
2	POW_LIMIT	R	0	--	Not supported and always set to 0.

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1	POUT_OPF	R	0	--	Not supported and always set to 0.
0	POUT_OPW	R	0	--	Not supported and always set to 0.

STATUS_INPUT (7Ch)

Format	N/A
Description	The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.
Default	00h

7	6	5	4	3	2	1	0
VIN_OVF	VIN_OVW	VIN_UVW	VIN_UVF	VIN_OFF	IIN_OCF	IIN_OCW	PIN_OPW
R	R-0	R-0	R	R-0	R	R	R-0

Bits	Field	Type	Reset	NVM	Description
7	VIN_OVF	R	--	--	Input Over-Voltage Fault 0: Latched flag indicating no VIN OV fault has occurred. 1: Latched flag indicating a VIN OV fault has occurred.
6	VIN_OVW	R	0	--	Not supported and always set to 0.
5	VIN_UVW	R	0	--	Not supported and always set to 0.
4	VIN_UVF	R	--	--	Input Under-Voltage Fault 0: Latched flag indicating no VIN UV fault has occurred. 1: Latched flag indicating a VIN UV fault has occurred.
3	VIN_OFF	R	--	--	Not supported and always set to 0.
2	IIN_OCF	R	0	--	Input Over-Current Fault 0: Latched flag indicating no IIN OC fault has occurred. 1: Latched flag indicating a IIN OC fault has occurred.
1	IIN_OCW	R	0	--	Input Over-Current Warning 0: Latched flag indicating no IIN OC warning has occurred. 1: Latched flag indicating a IIN OC warning has occurred.
0	PIN_OPW	R	0	--	Not supported and always set to 0.

STATUS_TEMPERATURE (7Dh)

Format	N/A
Description	The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.
Default	00h

7	6	5	4	3	2	1	0
OTF	OTW	UTW	UTF	Reserved			
R	R	R-0	R-0	R-0000			

Bits	Field	Type	Reset	NVM	Description
7	OTF	R	--	--	Over-Temperature Fault 0: Latched flag indicating no temperature fault has occurred. 1: Latched flag indicating a temperature fault has occurred.
6	OTW	R	--	--	Over-Temperature Warning 0: Latched flag indicating no temperature warning has occurred. 1: Latched flag indicating a temperature warning has occurred.
5	UTW	R	0	--	Not supported and always set to 0.
4	UTF	R	0	--	Not supported and always set to 0.

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3:0	Reserved	R	0000	--	Always set to 0.

STATUS_CML (7Eh)

Format	N/A
Description	The STATUS_ CML command returns one byte with contents regarding communication, logic, or memory conditions.
Default	00h

7	6	5	4	3	2	1	0
US_CMD	US_DATA	PEC_FAIL	MEM_FAULT	PRO_FAULT	Reserved	COM_FAIL	CML_OTHER
R	R	R	R	R-0	R-0	R	R-0

Bits	Field	Type	Reset	NVM	Description
7	US_CMD	R	--	--	Invalid or Unsupported Command Received 0: Latched flag indicating no invalid or unsupported command has received. 1: Latched flag indicating an invalid or unsupported command has received.
6	US_DATA	R	--	--	Invalid or Unsupported Data Received 0: Latched flag indicating no invalid or unsupported data has received. 1: Latched flag indicating an invalid or unsupported data has received.
5	PEC_FAIL	R	--	--	Packet Error Check Failed 0: Latched flag indicating no packet error check has failed 1: Latched flag indicating a packet error check has failed
4	MEM_FAULT	R	--	--	Memory Error 0: Latched flag indicating that there is no memory error. 1: Latched flag indicating that a memory error, i.e. PMBus controller is trying to write into registers when NVM memory is being programmed.
3	PRO_FAULT	R	0	--	Not supported and always set to 0.
2	Reserved	R	0	--	Always set to 0.
1	COM_FAIL	R	--	--	Other Communication Faults 0: Latched flag indicating no communication fault other than the ones listed in this table has occurred. 1: Latched flag indicating a communication fault other than the ones listed in this table has occurred.
0	CML_OTHER	R	0	--	Not supported and always set to 0.

STATUS_MFR_SPECIFIC (80h)

Format	N/A
Description	The STATUS_ MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.
Default	00h

7	6	5	4	3	2	1	0
MFR_FAULT_PS	MFR_PBF	CUR_SH_WARN			RST_VOUT	VOUT_MIN	PHFLT
R	R	R			R	R	R

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Bits	Field	Type	Reset	NVM	Description
7	MFR_FAULT_PS	R	--	--	Power State Fault 0: Latched flag indicating no fault from TI power stage has occurred. 1: Latched flag indicating a fault from TI power stage has occurred.
6	MFR_PBF	R	--	--	Pre-Bias Fault 0: Latched flag indicating no pre-bias fault (VOUT >2.75V at startup) has occurred. 1: Latched flag indicating a pre-bias fault (VOUT >2.75V at startup) has occurred.
5:3	CUR_SH_WARN	R	000	--	not supported and alwats set to 0
2	RST_VOUT	R	--	--	RST_VOUT Fault 0: Latched flag indicating no RST_VOUT fault has occurred. 1: Latched flag indicating a RST_VOUT fault has occurred.
1	VOUT_MIN	R	--	--	VOUT_MIN Fault 0: Latched flag indicating no VOUT_MIN fault has occurred. 1: Latched flag indicating a VOUT_MIN fault has occurred.
0	PHFLT	R	--	--	Phase Fault 0: Latched flag indicating no phase fault (no phase pulse detected) has occurred. 1: Latched flag indicating a phase fault (no phase pulse detected) has occurred.

READ_VIN (88h)

Format	Linear
Description	The READ_VIN command returns the input voltage in volts, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is a 5-bit, two's complement integer Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
READ_VIN_EXPONENT					READ_VIN_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_VIN_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_VIN_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_VIN_MANTISSA	R	--	--	11-bit, two's complement mantissa.

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READ_IIN (89h)

Format	Linear
Description	The READ_IIN command returns the input current in amperes, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is a 5-bit, two's complement integer Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
READ_IIN_EXPONENT					READ_IIN_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_IIN_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_IIN_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_IIN_MANTISSA	R	--	--	11-bit, two's complement mantissa.

READ_VOUT (8Bh)

Format	VID
Description	The READ_VOUT command returns the actual, measured output voltage.
Default	N/A

15	14	13	12	11	10	9	8
READ_VOUT_VID							
R							

7	6	5	4	3	2	1	0
READ_VOUT_VID							
R							

Bits	Field	Type	Reset	NVM	Description
15:0	READ_VOUT_VID	R	--	--	16-bit, VID format

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READ_IOUT (8Ch)

Format	Linear
Description	The READ_IOUT command returns the output current in amperes, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is a 5-bit, two's complement integer Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
READ_IOUT_EXPONENT					READ_IOUT_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_IOUT_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_IOUT_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_IOUT_MANTISSA	R	--	--	11-bit, two's complement mantissa.

READ_TEMPERATURE_1 (8Dh)

Format	Linear
Description	The READ_TEMPERATURE_1 command returns the temperature in degrees Celsius, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is a 5-bit, two's complement integer Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
READ_TEMP_1_EXPONENT					READ_TEMP_1_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_TEMP_1_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_TEMP_1_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_TEMP_1_MANTISSA	R	--	--	11-bit, two's complement mantissa.

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READ_TEMPERATURE_1 (8Dh)

Format	Linear
Description	The READ_TEMPERATURE_1 command returns the temperature in degrees Celsius, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is a 5-bit, two's complement integer Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
READ_TEMP_1_EXPONENT					READ_TEMP_1_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_TEMP_1_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_TEMP_1_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_TEMP_1_MANTISSA	R	--	--	11-bit, two's complement mantissa.

READ_POUT (96h)

Format	Linear
Description	The READ_POUT command returns the output power in watts, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is a 5-bit, two's complement integer Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
READ_POUT_EXPONENT					READ_POUT_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_POUT_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_POUT_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_POUT_MANTISSA	R	--	--	11-bit, two's complement mantissa.

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READ_PIN (97h)

Format	Linear
Description	The READ_PIN command returns the input power in watts. Refer to READ_PIN (97h) to get the real world value.
Default	N/A

15	14	13	12	11	10	9	8
READ_PIN_EXPONENT					READ_PIN_MANTISSA		
R					R		

7	6	5	4	3	2	1	0
READ_PIN_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:11	READ_PIN_EXPONENT	R	--	--	5-bit, two's complement exponent (scaling factor).
10:0	READ_PIN_MANTISSA	R	--	--	11-bit, two's complement mantissa.

PMBus_REVISION (98h)

Format	N/A
Description	The PMBus_REVISION command returns the revision of the PMBus to which the device is compliant.
Default	11h

7	6	5	4	3	2	1	0
PMBUS_REV							
R-0001 0001							

Bits	Field	Type	Reset	NVM	Description
7:0	PMBUS_REV	R	0001 0001	--	Compliant to revision 1.1 of the PMBus specification.

MFR_ID (99h)

Format	N/A
Description	The MFR_ID command loads the unit with the text character that contains the manufacturer's ID.
Default	5401h

15	14	13	12	11	10	9	8
MFR_ID_BW							
R/W							

7	6	5	4	3	2	1	0
MFR_ID_HC							
R-0000 0001							

Bits	Field	Type	Reset	NVM	Description
15:8	MFR_ID_BW	R/W	--	Yes	PMBus Block Write
7:0	MFR_ID_HC	R	0000 0001	--	Hard Coded to 01h

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MFR_MODEL (9Ah)

Format	N/A
Description	The MFR_MODEL command loads the unit with the text character that contains the model number of the manufacturer.
Default	4701h

15	14	13	12	11	10	9	8
MFR_MODEL_BW							
R/W							

7	6	5	4	3	2	1	0
MFR_MODEL_HC							
R-0000 0001							

Bits	Field	Type	Reset	NVM	Description
15:8	MFR_MODEL_BW	R/W	--	Yes	PMBus Block Write
7:0	MFR_MODEL_HC	R	0000 0001	--	Hard Coded to 01h

MFR_REVISION (9Bh)

Format	N/A
Description	The MFR_REVISION command loads the unit with the text character that contains the revision number of the manufacturer. This is typically done once at the time of manufacture.
Default	N/A

15	14	13	12	11	10	9	8
MFR_REVISION_HC1				MFR_REVISION_BW			
R-0000				R/W			

7	6	5	4	3	2	1	0
MFR_REVISION_HC2							
R-0000 0001							

Bits	Field	Type	Reset	NVM	Description
15:12	MFR_REVISION_HC1	R	0000	--	Hard Coded to 0h
11:8	MFR_REVISION_BW	R/W	--	Yes	PMBus Block Write
7:0	MFR_REVISION_HC2	R	0000 0001	--	Hard Coded to 01h

MFR_DATE (9Dh)

Format	N/A
Description	The MFR_DATE command loads the unit with the text character that identifies the device's date of manufacture. This is typically done once at the time of manufacture.
Default	N/A

15	14	13	12	11	10	9	8
MFR_DATE_BW							
R/W							

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7	6	5	4	3	2	1	0
MFR_DATE_HC							
R-0000 0001							

Bits	Field	Type	Reset	NVM	Description
15:8	MFR_DATE_BW	R/W	--	Yes	PMBus Block Write
7:0	MFR_DATE_HC	R	0000 0001	--	Hard Coded to 01h

MFR_VOUT_MIN (A4h)

Format	VID
Description	The MFR_VOUT_MIN command sets an lower limit on the output voltage that the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly non-operational level. The device detects that an attempt has been made to program the output to a voltage lower than the value set by the MFR_VOUT_MIN command. The device treats this detection as a warning condition and not a fault condition. If an attempt is made to program the output voltage lower than the limit set by this command, the device responds as follows: • The commanded output voltage is set to MFR_VOUT_MIN, • The OTHER bit is set in the STATUS_BYTE, • The VOUT bit is set in the STATUS_WORD, • The MFR_VOUT_MIN warning bit is set in the STATUS_VOUT register, and • The device notifies the host (asserts PMBUS_ALERT). The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols (VR12.0 or VR12.5) from the SLEW_MODE pin or MFR_SPECIFIC_13.
Default	0000h

15	14	13	12	11	10	9	8
RESERVED							
R-0000 0000							

7	6	5	4	3	2	1	0
MFR_VOUT_MIN							
R/W							

Bits	Field	Type	Reset	NVM	Description
15:8	RESERVED	R	0000 0000	--	Hard coded to 00h
7:0	MFR_VOUT_MIN	R/W	0000 0000	--	Minimum value for VID

MFR_SPECIFIC_00 (Per-Phase Overcurrent Limit) (D0h)

Format	N/A
Description	The MFR_SPECIFIC_00 command sets the valley-current threshold for the perphase overcurrent limit.
Default	0Fh

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7	6	5	4	3	2	1	0
Reserved				OCL			
R-0000				R/W			

Bits	Field	Type	Reset	NVM	Description
7:4	Reserved	R	R-0000	--	Always set to 0.
3:0	OCL	R/W	--	Yes	0000: 24A 0001: 27A 0010: 30A 0011: 33A 0100: 36A 0101: 39A 0110: 42A 0111: 45A 1000: 48A 1001: 51A 1010: 54A 1011: 57A 1100: 60A 1101: 63A 1110: 66A 1111:69A

MFR_SPECIFIC_01 (Telemetry Averaging Time) (D1h)

Format	N/A
Description	The MFR_SPECIFIC_01 command sets the averaging time for telemetry reporting.
Default	50h

7	6	5	4	3	2	1	0
Reserved	FILTER_PIN			Reserved		FILTER_IV	
R-0	R/W			R-00		R/W	

Bits	Field	Type	Reset	NVM	Description
7	Reserved	R	0	--	Always set to 0.
6:4	FILTER_PIN	R/W	101	--	Averaging Time for Input Power Reporting 000: Bypass. 001: 2 ms 010: 5.5 m 011: 11.5 m 100: 19 ms 101: 50 ms 110: 100 ms 111: 225 ms
3:2	Reserved	R	00	--	Always set to 0.
1:0	FILTER_IV	R/W	00	--	Averaging Time for Current and Voltage Reporting 00: Bypass. 01: .5 ms 10: 1 ms 11: 2.5 ms

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MFR_SPECIFIC_04 (Read VOUT) (D4h)

Format	Linear
Description	The MFR_SPECIFIC_04 command returns the actual, measured output voltage in volts, shown in below equation. $X = Y \times 2^N$ • X is the real world value • Y is an 11-bit, two's complement integer • N is -9 Note that devices that use the Linear format must accept and be able to process any value of N.
Default	N/A

15	14	13	12	11	10	9	8
MFR_SPEC_04_MANTISSA							
R							

7	6	5	4	3	2	1	0
MFR_SPEC_04_MANTISSA							
R							

Bits	Field	Type	Reset	NVM	Description
15:0	MFR_SPEC_04_MANTISSA	R	--	--	Unsigned 16-bit mantissa with an exponent value of n=-9.

MFR_SPECIFIC_05 (VOUT Trim) (D5h)

Format	Signed Two's Complement
Description	The MFR_SPECIFIC_05 command is used to trim the VR output voltage in volts. LSB resolution is 5 mV/10 mV based on the selected VR12.0/VR12.5.
Default	00h

7	6	5	4	3	2	1	0
VOUT_VID_OFFSET							
R/W							

Bits	Field	Type	Reset	NVM	Description
7:0	VOUT_VID_OFFSET	R/W	--	Yes	Sets the VR output trim voltage. 01111111: 0.635 V in VR12.0 and 1.27V in VR12.5 01111110: 0.630 V in VR12.0 and 1.26 V in VR12.5 ..... 00000001: 0.005 V in VR12.0 and 0.01 V in VR12.5 00000000: 0 V 11111111: –0.005 V in VR12.0 and –0.01 V in VR12.5 ..... 10000001: –0.635 V in VR12.0 and –1.27 V in VR12.5 10000000: –0.640 V in VR12.0 and –1.28 V in VR12.5

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MFR_SPECIFIC_07 (Additional Function Bits) (D7h)

Format	N/A
Description	The MFR_SPECIFIC_07 command sets the additional function bits.
Default	03h

7	6	5	4	3	2	1	0
Reserved					SLEW_FAST	OSR_TRISTATE	SST_TIME
R-0000 0					R/W		

Bits	Field	Type	Reset	NVM	Description
7:3	Reserved	R	000 00	--	Always set to 0.
2	SLEW_FAST	R/W	--	Yes	Fast Slew Mode Enable/Disable 0: Default slew rate selected by MFR_SPECIFIC_13(2:0) 1: Add 1.36 mV/μs to the selected slew rate
1	OSR_TRISTATE	R/W	--	Yes	Body Braking Enable/Disable 0: Enable OSR pulse truncation without body braking 1: Enable OSR pulse truncation with body braking
0	SST_TIME	R/W	--	Yes	Soft Slew Rate Selection 0: soft start slew rate dependent on TRISE 1: 1/16 of the selected slew rate for soft-start

MFR_SPECIFIC_08 (Droop) (D8h)

Format	N/A
Description	The MFR_SPECIFIC_08 command sets the load line as percentage of the default one. For example, if slope is set as 1mohm = 100%, then 0.5mohm = 50%
Default	04h

7	6	5	4	3	2	1	0
DROOP							
R/W							

Bits	Field	Type	Reset	NVM	Description
7:0	DROOP	R/W	0000 0100	--	0000 0000: 0% 0000 0001: 25% 0000 0010: 50% 0000 0011: 75% 0000 0100: 100% 0001 0000: 80% 0010 0000: 85% 0011 0000: 90% 0100 0000: 95% 0101 0000: 105% 0110 0000: 110% 0111 0000: 115% 1000 0000: 120% 1001 0000: 125% 1010 0000: 150% 1011 0000: 175% Others: 100%

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MFR_SPECIFIC_09 (OSR/USR) (D9h)

Format	N/A
Description	The MFR_SPECIFIC_09 command sets the threshold for OSR and USR control.
Default	77h

7	6	5	4	3	2	1	0
Reserved	USR			Reserved	OSR		
R-0	R/W			R-0	R/W		

Bits	Field	Type	Reset	NVM	Description
7	Reserved	R	0	--	Always set to 0.
6:4	USR	R/W	--	Yes	Undershoot Reduction 000: 20 mV 001: 30 mV 010: 60 mV 011: 80 mV 100: 100 mV 101: 120 mV 110: 140 mV 111: USR off
3	Reserved	R	0	--	Always set to 0.
2:0	OSR	R/W	--	Yes	Overshoot Reduction 000: 30 mV 001: 40 mV 010: 60 mV 011: 80 mV 100: 100 mV 101: 120 mV 110: 140 mV 111: OSR off

MFR_SPECIFIC_10 (Maximum Operating Current) (DAh)

Format	N/A
Description	The MFR_SPECIFIC_10 command sets the maximum operating current (IMAX, unit: A) of the converter.
Default	E9h

7	6	5	4	3	2	1	0
IMAX							
R/W							

Bits	Field	Type	Reset	NVM	Description
7:0	IMAX	R/W	--	Yes	Set maximum operating current.

MFR_SPECIFIC_11 (VBOOT) (DBh)

Format	VID
Description	The MFR_SPECIFIC_11 command sets the boot voltage in 8-bit VID format.
Default	97h

7	6	5	4	3	2	1	0
VBOOT							
R/W							

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Bits	Field	Type	Reset	NVM	Description
7:0	VBOOT	R/W	--	Yes	Set the boot voltage according to the selected VID table.

MFR_SPECIFIC_12 (Switching Frequency and TRISE) (DCh)

Format	VID
Description	The MFR_SPECIFIC_12 command sets the switching frequency and the soft start rise slew rate.
Default	00h

7	6	5	4	3	2	1	0
FSW				Reserved		TRISE	
R/W				R-0		R/W	

Bits	Field	Type	Reset	NVM	Description
7:4	FSW	R/W	--	Yes	Switching Frequency 0000: 300 kHz 0001: 400 kHz 0010: 500 kHz 0011: 600 kHz 0100: 700 kHz 0101: 800 kHz 0110: 900 kHz 0111: 1000 kHz 1000: 350 kHz 1001: 450 kHz 1010: 550 kHz 1011: 650 kHz 1100: 750 kHz 1101: 850 kHz 1110: 950 kHz 1111: 1000 kHz
3:2	Reserved	R	0	--	Always set to 0.
1:0	TRISE	R/W	--	Yes	Soft start rise slew rate in terms of VOUT slew rate 00: 1 01: 1/2 10: 1/4 11: 1/8

MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) (DDh)

Format	N/A
Description	The MFR_SPECIFIC_13 command sets the slew rates and the operation modes.
Default	88h

7	6	5	4	3	2	1	0
VR12_MODE	PI_SET	Reserved	DPS_EN	ZLL_SET	SLEW		
R/W	R/W	R/W	R/W	R/W	R/W		

Bits	Field	Type	Reset	NVM	Description
7	VR12_MODE	R/W	--	Yes	VR12 Mode 0: VR12.5. 1: VR12.0.
6	PI_SET	R/W	--	Yes	Phase Interleaving 0: 4 phase interleaving individually. 1: 1/3 and 2/4 two phase interleaving
5	Reserved	R/W	--	Yes	Not used, write or read has no effect
4	DPS_EN	R/W	--	Yes	Dynamic Phase Shedding Enable 0: Disable dynamic phase shedding. 1: Enable dynamic phase shedding.

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3	ZLL_SET	R/W	--	Yes	Load Line 0: Non-zero load line 1: Zero load line
2:0	SLEW	R/W	--	Yes	Slew Rate 000: 0.34 mV/μs 001: 0.68 mV/μs 010: 1.02 mV/μs 011: 1.36 mV/μs 100: 1.7 mV/μs 101: 2.04 mV/μs 110: 2.38 mV/μs 111: 2.74 mV/μs

MFR_SPECIFIC_14 (Ramp Height) (DEh)

Format	N/A
Description	The MFR_SPECIFIC_14 command sets the ramp amplitude for compensations.
Default	06h

7	6	5	4	3	2	1	0
Reserved					RAMP		
R-0000 0					R/W		

Bits	Field	Type	Reset	NVM	Description
7:3	VR12_MODE	R	0	--	Always set to 0.
2:0	PI_SET	R/W	--	Yes	Ramp Amplitude 000: 20 mV_{PP} 001: 40 mV_{PP} 010: 60 mV_{PP} 011: 80 mV_{PP} 100: 100 mV_{PP} 101: 120 mV_{PP} 110: 150 mV_{PP} 111: 200 mV_{PP}

MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) (DFh)

Format	N/A
Description	The MFR_SPECIFIC_15 command sets the threshold for the dynamic phase shedding. Use 4 x overcurrent limit (OCL) as 100% load condition
Default	01h

7	6	5	4	3	2	1	0
Reserved				DPS_TH_LOW	DPS_TH_HIGH		
R-0000				R/W	R/W		

Bits	Field	Type	Reset	NVM	Description
7:4	Reserved	R	0000	--	Always set to 0.
3	DPS_TH_LOW	R/W	--	Yes	Switch from 2 Phase to 1 Phase Operation 0: Disable decreasing to 1 phase operation. 1: 10% load.
2:0	DPS_TH_HIGH	R/W	--	Yes	Switch from 4 Phase to 2 Phase Operation 000: 15% load. 001: 20% load. 010: 25% load. 011: 30% load. Others: 35% load.

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MFR_SPECIFIC_16 (VIN UVLO) (E0h)

Format	N/A
Description	The MFR_SPECIFIC_16 command sets the threshold for the VIN Undervoltage Lockout (UVLO).
Default	00h

7	6	5	4	3	2	1	0
Reserved						VIN_UVLO	
R-00 0000						R/W	

Bits	Field	Type	Reset	NVM	Description
7:2	Reserved	R	00 0000	--	Always set to 0.
1:0	VIN_UVLO	R/W	01	Yes	Input Voltage UVLO 00: 4.5 V 01: 7.25 V 10: 9.0 V 11: 10.3 V

MFR_SPECIFIC_20 (Maximum Operational Phase Number) (E4h)

Format	N/A
Description	The MFR_SPECIFIC_20 command sets the maximum operational phase numbers on-the-fly. If the maximum operational phase number is set higher than the available phase numbers specified by hardware, then the operational phase number remains unchanged, and the STAUTS_MFR_SPECIFIC<3> is set while asserting PMB_ALERT.
Default	Hardware Specific

7	6	5	4	3	2	1	0
Reserved					PHASE_NUM		
R-0 0000					R/W		

Bits	Field	Type	Reset	NVM	Description
7:3	Reserved	R	0 0000	--	Always set to 0.
2:0	PHASE_NUM	R/W	--	--	Phase Number 000: 1-phase operation. 001: 2-phase operation. 010: 3-phase operation. 011: 4-phase operation. 100: 5-phase operation. 101: 6-phase operation. Others: N/A

MFR_SPECIFIC_22 (VOUT_UV_FAULT_threshold) (E6h)

Format	N/A
Description	The MFR_SPECIFIC_22 command sets the value of VOUT undervoltage threshold. UVP threshold = VOUT_COMMAND - VOUT_UVF_OFFSET
Default	03h

7	6	5	4	3	2	1	0
Reserved					VOUT_UVF_THRESHOLD		
R-0 0000					R/W		

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Bits	Field	Type	Reset	NVM	Description
7:3	Reserved	R	0 0000	--	Always set to 0.
2:0	VOUT_UVF_THRESHOLD	R/W	--	Yes	VOUT UVF threshold 000: 50 mV 001: 100 mV 010: 150 mV 011: 200 mV 100: 250 mV 101: 300 mV 110: 325 mV 111: 400 mV

MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)

Format	N/A
Description	The MFR_SPECIFIC_44 command reads back the DEVICE_CODE information.
Default	01F0h

15	14	13	12	11	10	9	8
DEVICE_CODE							
R-0000 0001							

7	6	5	4	3	2	1	0
DEVICE_CODE							
R-1111 0000							

Bits	Field	Type	Reset	NVM	Description
15:0	DEVICE_CODE	R	0000 0001 1111 0000	--	Device Code

注：

1. 包装信息请参见《产品出货包装信息》，载带卷盘包装包编号：58210321；
2. 最大容性负载均在输入电压范围、满负载条件下测试；
3. 除特殊说明外，本手册所有指标都在 Ta=25℃，湿度<75%RH，标称输入电压和正输出额定负载时测得；
4. 本手册所有指标的测试方法均依据本公司企业标准；
5. 我司可提供产品定制，具体需求可直接联系我司技术人员；
6. 产品涉及法律法规：见“产品特点”；
7. 我司产品报废后需按照 ISO14001 及相关环境法律法规分类存放，并交由有资质的单位处理。

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