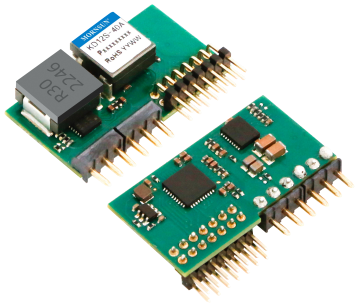
非隔离稳压 40A 单路输出，POL 数字模块电源



专利保护 RoHS

- ASICs、FPGA、ARM
- 网络处理器
- AI 处理器
- 分布式电源
- 通信设备
- 服务器和储存设备

产品特点

- 宽输入电压范围：4.5-14VDC，含 5V、12V 通用输入
- 输出电压可调：0.6V-3.3VDC
- 40A 输出电流
- 高精度产品输出电压偏差 3mV
- 输出纹波低至 6 mVp-p，0.6Vout，100%Io
- PMBus 数字通信协议
- 工作温度范围：-40 ℃ to +85 ℃
- 效率高达 96.7%，5Vin，3.3Vout，50%Io，损耗仅 4.5W
- 具备远程控制、PGOOD、远端补偿、时钟同步功能
- 具备输入欠压、输出过/欠压保护功能
- 具备输出过流、短路、过温保护功能
- 通过 PMBus 进行配置和监控

KD12S-40A 是一款非隔离 40A 单路输出的 POL 数字模块电源，它可工作在 4.5-14VDC 的宽输入电压范围，兼容前端 5V/12V 输入系统，并通过外部模拟分压和 PMBus 数字控制，提供精确可调的 0.6-3.3VDC 电压的输出；另外它还具备 PMBus① 通信协议、远程控制、PGOOD、远端补偿、时钟同步的功能，并具备输入过/欠压、输出过/欠压、输出过流、短路、过温等保护，上位机可实现人机交互，提供大量操作指令去控制和监控模块，同时它拥有高电压精度、低输出纹波、高动态响应等特性。

注：①搭配使用我司上位机，详情见我司官网，技术支持可咨询我司 FAE。

选型表

认证	产品型号	输入电压 (VDC) 标称值 (范围值)	输出电压① (VDC)	输出电流 (A.) 最大值	输出电压偏差 (mV) 标称值	效率 （标称，满载，典型值）	纹波 （Vo=1.0VDC） 标称满载
--	KD12S-40A	12 （4.5-14）	（0.6-1.8）	40	±3	87.5%（Vo=1.0VDC）	12mVp-p
		5-7.5	3.3	30			
		12 （7.5-14）		40			

注：
①模块出产设置默认输出 0.6V 输出，阈值微调具体调节见 PMBus 操作指南，模拟调节见 Trim 调节功能。

极限额定值

参数		Min.	Max.	单位
电压	VIN	-0.3	15	V
	NC、TRIM、PG、CTRL、SHARE3、SHARE1	-0.3	7	
	VS-、VS+、DATA、SMBALERT#、CLK、SYNC、SHARE、SHARE2	-0.3	5.5	
	ADDRESS 0、ADDRESS 1	-0.3	3.6	

注：
1.若超出“最大额定值”表内列出的应力值，可能会对器件造成永久损坏。长时间工作在极限额定条件下，器件的可靠性有可能会受到影响。所有电压值都是以大地(GND)为参考基准。
2.该电源模块可应用于多种应用，从简单的独立供电到复杂的分布式电源架构，为了保持其最大的灵活性，内部不包含保险丝，但是为了实现系统最大的安全性和系统保护，推荐输入端增加保险丝（最大额定值推荐为 35A），也可根据实际应用需求，选择适合的保险丝。

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电气特性

项目	工作条件/参数		Min.	Typ.	Max.	单位
输入电压范围			4.5	12	14	VDC
输出电压范围	通过外置电阻分压器		0.6	--	3.3	
最大输入电流	100%负载		--	20.6	--	A
最大输出电流			--	--	40	
输出过流保护阈值（可通过 PMBus 调节）	0.6-3.3		--	50	--	
空载输入电流	标称输入电压、0%负载，Vo=0.6V		--	30	--	mA
（模块使能）	标称输入电压、0%负载，Vo=3.3V		--	220	--	
输出电压偏差			--	3	20	mV
线性调整偏差			--	1	6	
负载调整偏差	按 10%Io-100%Io 测试		--	2	10	
输出电压纹波&噪声	20MHz，靠测法	0.6VDC	--	6	--	mVp-p
		1.0VDC	--	12	--	
		1.8VDC	--	18	--	
		3.3VDC	--	33	--	
动态负载	20MHz，靠测法 25%-75%负载阶跃变化，标称输入电压 Co=6x47uf+2x680uF+4x100uF	0.6VDC	--	±18	±85	mV
		1.0VDC	--	±36	±110	
		1.8VDC	--	±54	±150	
		3.3VDC	--	±99	±240	
温度漂移系数			--	±0.4	--	%/℃
最大容性负载			--	--	10000	μF
效率	Vin=12VDC，100%负载	Vo=0.6VDC	79.4	81.4	--	%
		Vo=1.0DC	85.5	87.5	--	
		Vo=1.8VDC	89.7	91.7	--	
		Vo=3.3VDC	92	94.3	--	
损耗	Vin=12VDC，100%负载	Vo=0.6VDC	--	5.48	--	W
		Vo=1.0VDC	--	5.71	--	
		Vo=1.8VDC	--	6.52	--	
		Vo=3.3VDC	--	7.98	--	
模块频率			--	540	--	kHz
时钟同步/SYNC	同步时钟范围		200	--	1500	
	高电平		2.0	--	--	V
	低电平		--	--	0.8	V
	最小脉冲宽度		--	--	100	ns
远程控制正逻辑 CTRL	高电平（模块开）		2.1	--	5	V
	低电平（模块关）		0	--	0.5	
远程控制负逻辑 CTRL	高电平（模块关）		2.1	--	5	
	低电平（模块开）		0	--	0.5	
输入欠压保护	开启阈值		--	4.25	--	V
	关断阈值		--	4.0	--	
	PMBus 指令可调范围		4.25	--	14	
输出过压保护	TRIM 阈值		--	800	--	mV
输出欠压保护	TRIM 阈值		--	528	--	mV

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输出过温保护		--	130	--	℃
热插拔		不支持			

注：
1.本模块采用数字控制，数字控制包含一个配置文件，修改配置文件会影响模块的功能和性能。除非另有说明，所有规格均为在默认配置文件下的规格，如需更改配置文件，可参考以下 PMBus 指令信息，同理上表模块正负逻辑通过数字控制修改；
2.除非另有说明，以上规格均在设计参考推荐外围下测试得出；
3.除非另有说明，输出电压的测试均在产品输出引脚上进行；
4. 除非另有说明，以上规格均适用 1.0V 输出；
5.更改开关频率会影响模块性能，更改前请与 FAE 确认；
6.外部同步时钟引脚信号必须是占空比为 50%的方波。
7.3. 3V 线性调节率低压以 7. 5V 为准；

PMBus 数字特性

项目	工作条件	Min.	Typ.	Max.	单位
上位机信号特性					
过温保护		--	130	--	℃
PMBus 温度调节范围		120	--	160	
输入欠压保护 PMBus 可调范围		4.25	--	13.8	V
PGOOD 特性					
PGOOD 阈值精度		-4	--	4	%
上位机测量特性					
上位机输出电压测量范围		0.5	--	4.5	V
上位机输出电压偏置电压		--	0.1	--	
上位机输出电压测量精度	Vo=1V	-0.8	--	0.8	%
上位机输出电流测量范围		0	--	50	A
上位机输出电流测量偏差	Io≥20A，IOUT_CAL_GAIN=0.503mΩ	-640	--	640	mA
注：以上内容为 PMBus 数字配置相关规格，其具体应用见应用推荐。					
输入欠压保护					
$V_{IN(on)}$	输入欠压开启电压	默认值	--	4.25	--	V
$V_{IN(off)}$	输入欠压关断电压	默认值	--	4	--	
$V_{INON(rng)}$	输入欠压开启电压可配置范围		4.25	--	14	
$V_{INOFF(rng)}$	输入欠压关断电压可配置范围		4	--	13.75	
注：输入欠压回差至少设置在 150mV 以上。					
输出过压/欠压保护					
V_{TrimOV}	Trim 过压阈值	默认值	--	800	--	mV
V_{TrimUV}	Trim 欠压阈值	默认值	--	528	--	
注：Trim 基准电压为 600mV，Trim 电压未达到 800mV 之前，产品关断驱动，但不进入过压保护状态（锁存关断），Trim 电压达到 800mV，产品锁存关断。					
PGOOD					
$V_{TrimPGH}$	PGOOD 高电平阈值	默认值	--	642	--	mV
$V_{TrimPGL}$	PGOOD 低电平阈值	默认值	--	558	--	
$V_{PG(acc)}$	PGOOD 阈值配置精度		-4	--	4	%
$V_{PG(hyst)}$	PGOOD 回差电压		15	28	45	mV
R_{PGOOD}	PGOOD 内部下拉电阻	V_{Trim}=0V， I_{PGOOD}=5mA	--	50	--	Ω
$I_{PGOOD(lk)}$	PGOOD 引脚漏电流	V_{Trim} = 600 mV， V_{PGOOD} = 5 V	--	--	20	μA
$t_{PGDELAY}$	PGOOD 延迟时间（软启动完成后）	默认值	--	2	--	ms

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通用特性

项目	工作条件	Min.	Typ.	Max.	单位
工作温度	见温度降额曲线图	-40	--	85	℃
存储温度		-55	--	125	
存储湿度	无凝结	5	--	95	%RH
回流焊温度*		峰值温度 Tc≤260℃，217℃以上时间最大为 60 s			
平均无故障时间（MTBF）	MIL-HDBK-217F@25℃	18957	--	--	k hours
海拔高度		--	--	2000	m
振动		10-150Hz, 5G, 0.75mm. along X, Y and Z			
潮敏等级(MSL)	IPC/JEDEC J-STD-020D.1	MSL 3			
污染等级		PD 3			

注：*实际应用请参考 IPC/JEDEC J-STD-020D.1 标准。

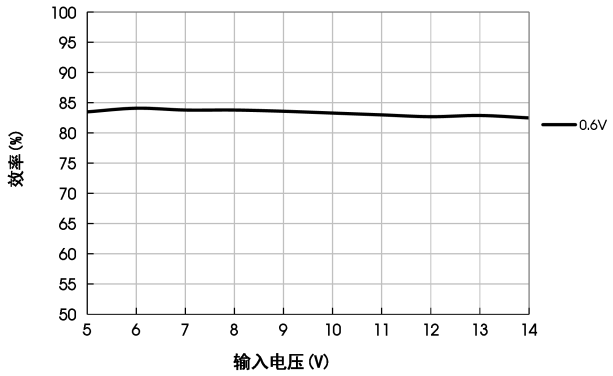
物理特性

外壳材料	开板
封装尺寸	33.00 x 22.10 x 9.05 mm
重量	8.8g(Typ)
冷却方式	自然空冷或强制风冷

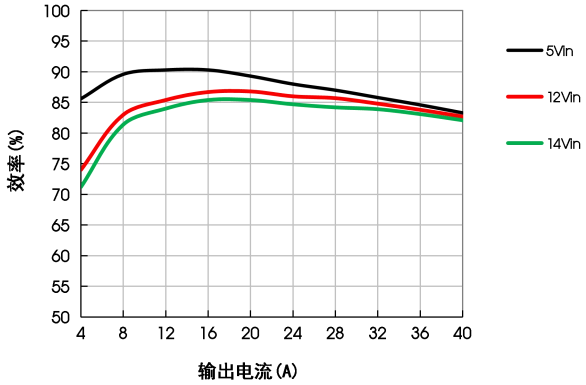
曲线特性

以下图示提供一个典型特征曲线（0.6V 输出，25℃）

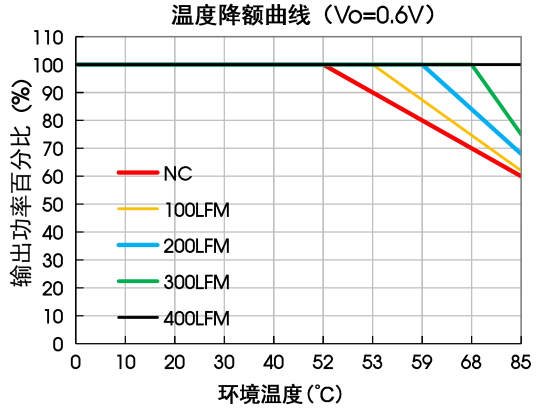
效率Vs输入电压（满载）

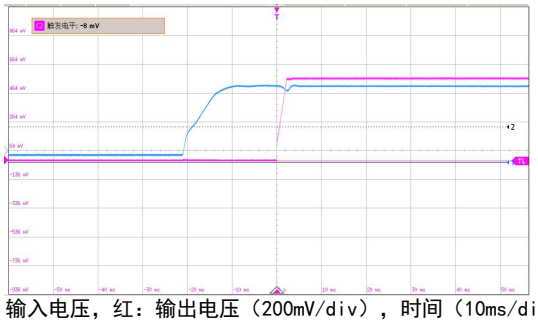


效率Vs输出负载（Vout=0.6V）



温度降额曲线（Vo=0.6V）





蓝：输入电压，红：输出电压（200mV/div），时间（10ms/div）

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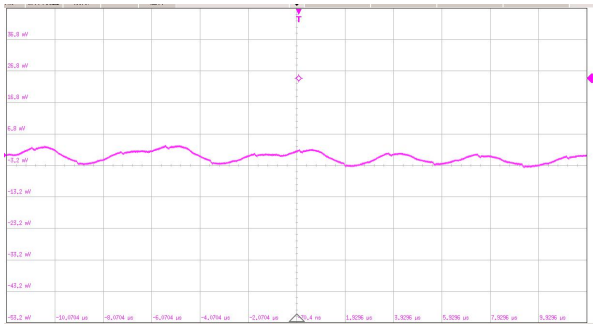
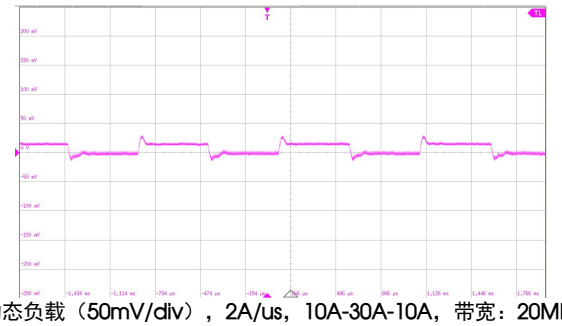


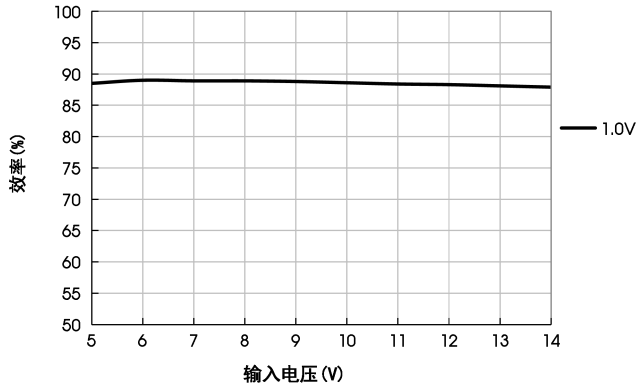
输出纹波&噪声（10mV/div），带宽：20MHz



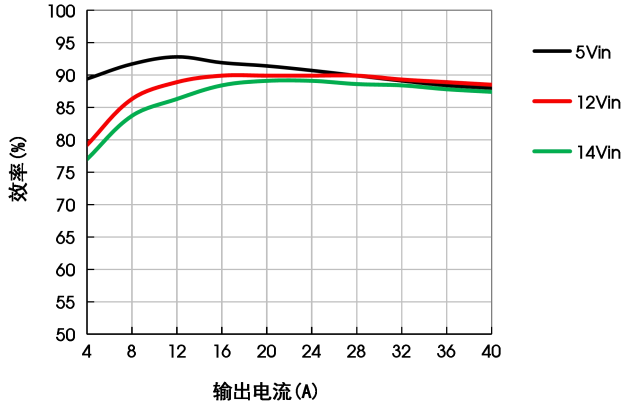
动态负载（50mV/div），2A/us，10A-30A-10A，带宽：20MHz

以下图示提供一个典型特征曲线（1.0V 输出，25℃）

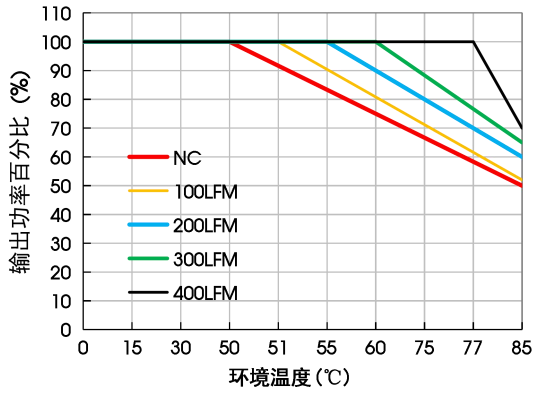
效率Vs输入电压（满载）

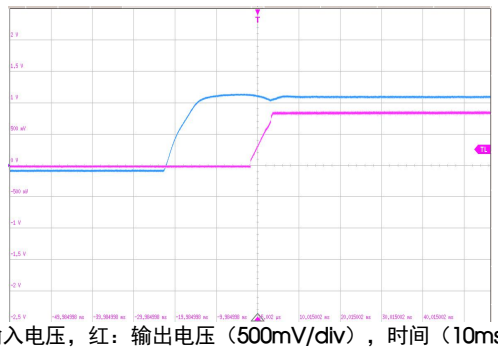


效率Vs输出负载（Vout=1.0V）

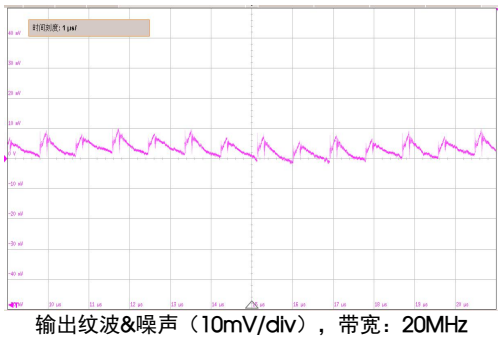


温度降额曲线（Vo=1.0V）

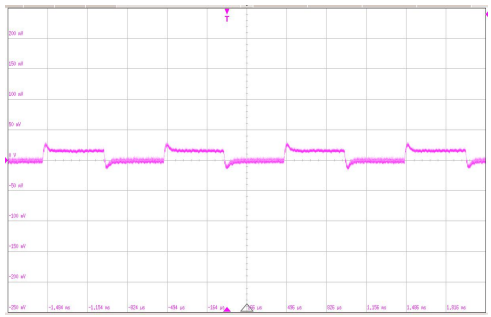




蓝：输入电压，红：输出电压（500mV/div），时间（10ms/div）



输出纹波&噪声（10mV/div），带宽：20MHz



动态负载（50mV/div），2A/us，10A-30A-10A 带宽：20MHz

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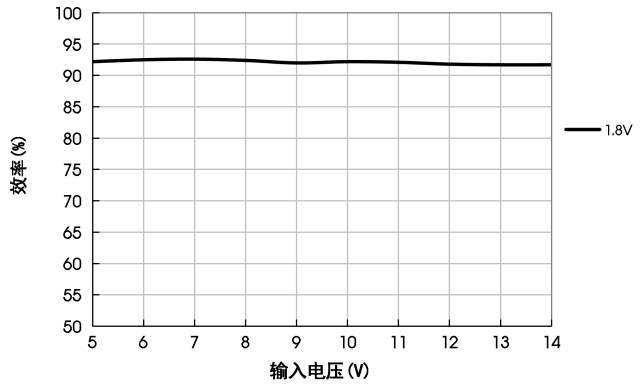
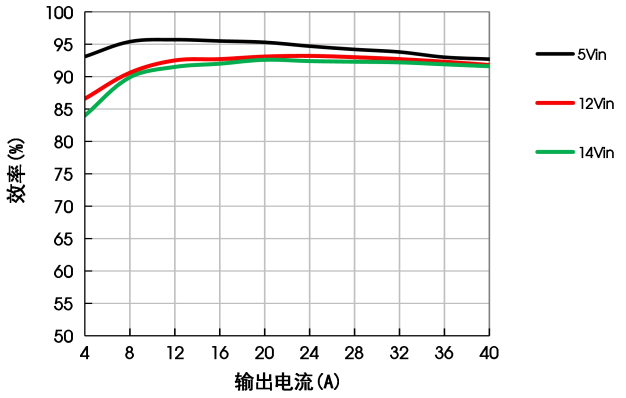
以下图示提供一个典型特征曲线（1.8V 输出，25℃）

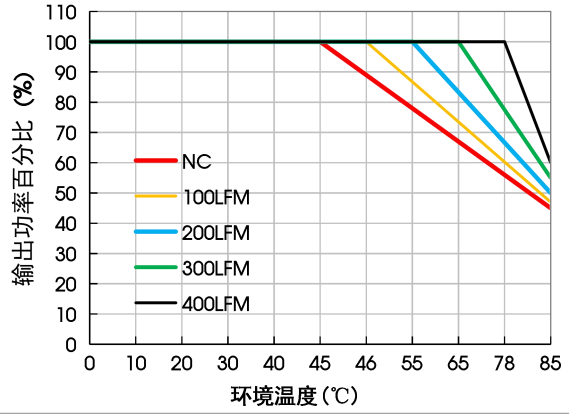
效率Vs输入电压（满载）

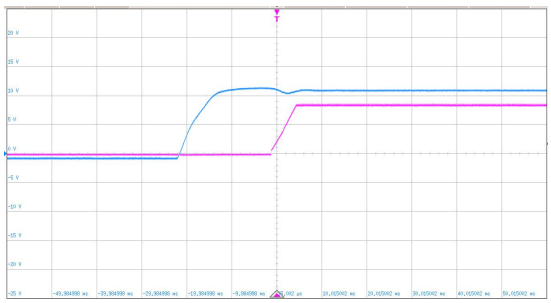


效率Vs输出负载（Vout=1.8V）

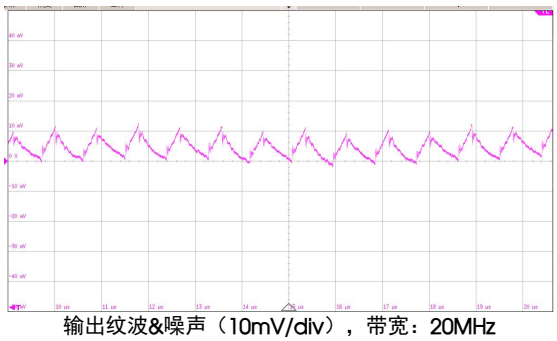


温度降额曲线（Vo=1.8V）

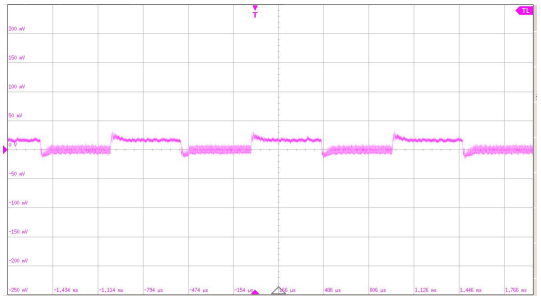




蓝：输出电压，红：输入电压（1000mV/div），时间（10ms/div）



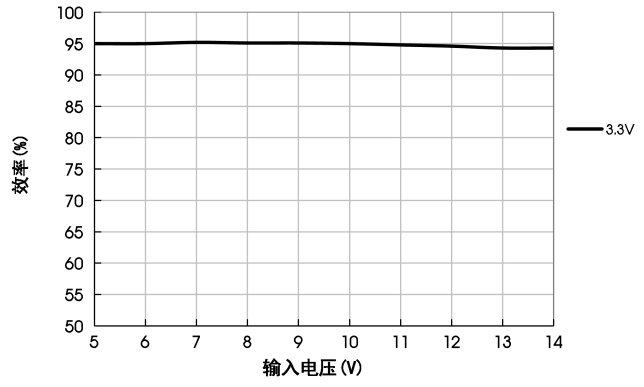
输出纹波&噪声（10mV/div），带宽：20MHz



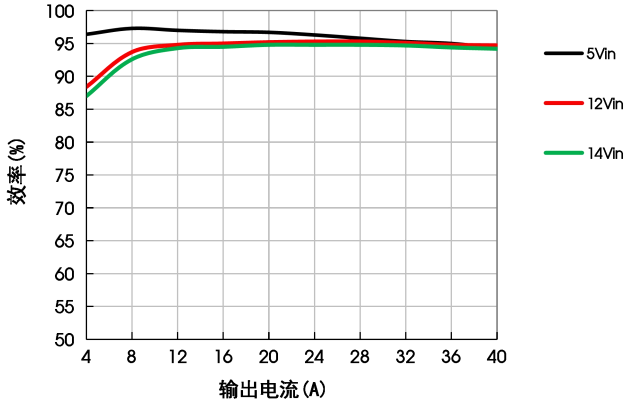
动态负载（50mV/div），2A/us，10A-30A-10A 带宽：20MHz

以下图示提供一个典型特征曲线（3.3V 输出，25℃）

效率Vs输入电压（满载）



效率Vs输出负载（Vout=3.3V）



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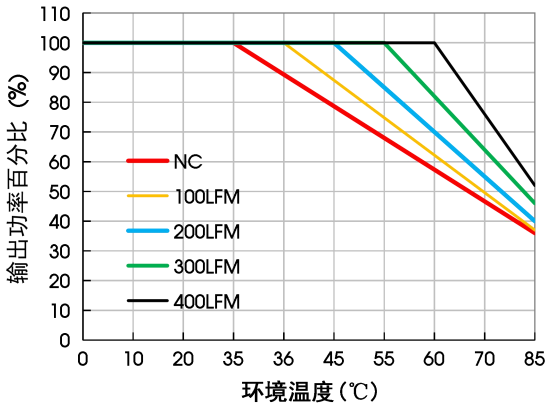
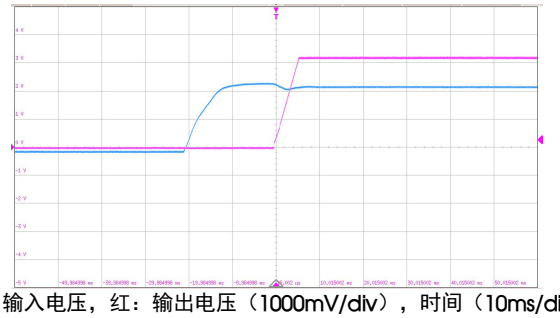
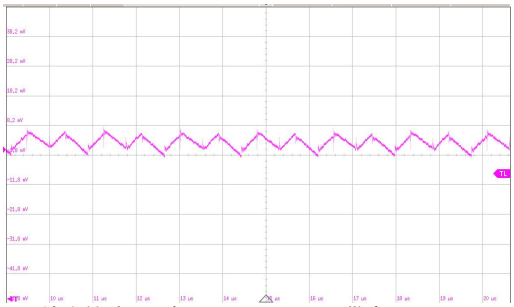
温度降额曲线（Vo=3.3V）

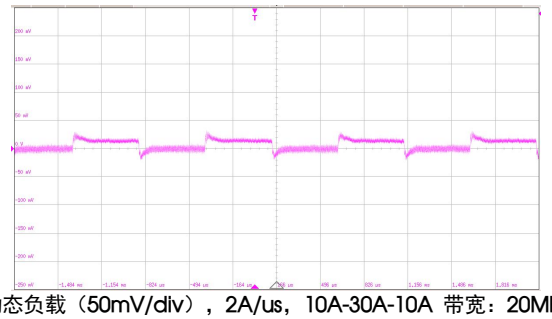




蓝：输入电压，红：输出电压（1000mV/div），时间（10ms/div）



输出纹波&噪声（10mV/div），带宽：20MHz



动态负载（50mV/div），2A/us，10A-30A-10A 带宽：20MHz

输入滤波

该模块应该接入一个低交流阻抗电源，必须保证一个输入电容靠近模块输入引脚附近，确保模块稳定；为了最小化输入电压纹波，推荐使用低 ESR 的陶瓷电容和低 ESR 的电解/聚合物电容。

如应用于 4.5V 输入应用时，请按以下建议进行：

a、前级输入必须保证电压≥4.5V；

B、对于前端 PCB layout 推荐：建议使用至少 4oz，宽度大于 1cm，长度小于 5cm。

输出纹波噪声

默认的环路补偿可以适应大多数的应用需求。另外产品输出会有一部分低频纹波干扰，这种低频纹波与控制环路的不稳定无关，模块总输出纹波和噪声可以保持在一个较低的幅值。

建议将低 ESR 的陶瓷电容和低 ESR 的电解/聚合物电容放置在尽可能靠近负载的位置，并且并联多个电容以降低其 ESR。为了使电容更有效，建议应用时关注 PCB 布局和布线。

输出精度

该模块为高精度产品，以下为输出电流 0-40A，输出电压 1.0VDC，4.5-14VDC 输入，典型精度曲线：

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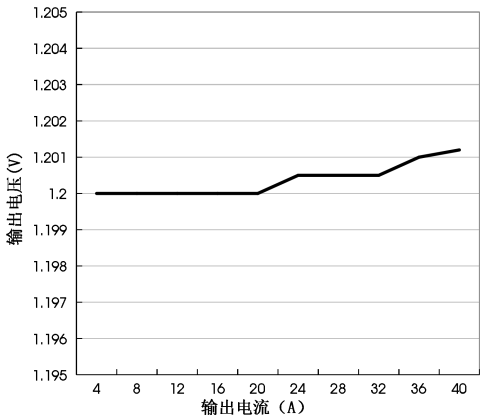
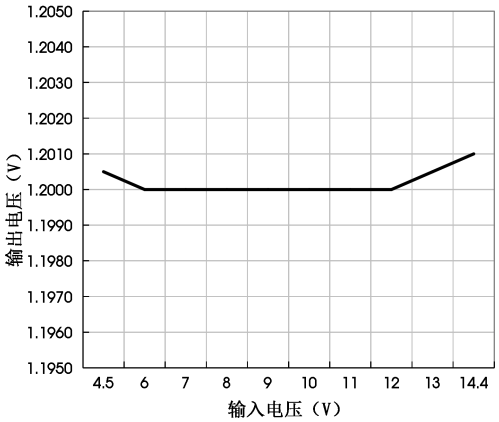


负载调节偏差



线性调节偏差

PMBus 数据格式

PMBus 数据格式

PMBus 命令（设置阈值、电压或者异常状态）支持三种数据格式，它们需要以文字数字表示作为参数(设置阈值、电压或报告此类命令)。兼容模块只需要支持其中一种格式即可。模块仅支持这些命令的线性数据格式。在这种格式中，data 参数由尾数和指数两部分组成。该参数表示的数字可以表示为:

$$数值=尾数 \times 2^{指数}$$

PMBus 地址位

在总线上，每个电源模块必须分配唯一的地址，通过 ADDRESS 1 和 ADDRESS 0 引脚可选择 64 个地址（0-63），地址以两个八进制（0-7）数字（以十进制表示的 0 到 63）的形式设置，每个引脚一个数字，ADDRESS 1 是高阶数字，ADDRESS 0 是低阶数字，PMBus 通信时，模块电源的 PMBus 地址位 ‘0b’ +ADDRESS 1+ADDRESS 0，地址设置电阻如下表：

数字	电阻(kΩ)
0	8.45
1	16.2
2	25.5
3	37.4
4	54.9
5	84.5
6	133
7	200

例如：
ADDRESS 1 使用 37.4K 电阻，ADDRESS 0 使用 37.4K 电阻，八进制数值为 33，实际上位机显示 27 地址位
注意：
1、若 ADDRESS 1 和 ADDRESS 1 引脚电阻超出范围值，电源模块不会继续响应 PMBus 指令，上位机不会显示模块被检测；
2、使用其他阻值可能会导致 PMBus 地址不正确，建议确保阻值与上表符合。

模块的开机和关机

模块的开机和关机由 PMBus 操作指令、远程控制引脚和输入电压共同控制（可以通过 PMBus 指令设置启机延迟和关机延迟时间）。

注意事项：
1.如果模块运行在关机延迟时间内，应避免在关机延迟时间之前再开启模块，只有在关机延迟时间结束且模块关闭后，模块才被允许打开，对于两模块并联应用也是如此，两个模块的开关延迟时间必须配置为相同的值。

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软启动

模块可配置软启动时间，由 TON_RISE PMBus 命令从 600 us 到 9 ms 可选配置，详细信息可参阅命令说明。在选择软启动时间时，应考虑输出电容上的充电电流，在有大量输出电容的应用下，这种电流会导致过流保护而关断模块。故为确保这些问题不会发生，在考虑过流阈值设置时，应考虑输出电容的充电电流。输出电容的充电电流由下式可得:

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}}$$

•ICAP 为输出电容的充电电流，单位为 A

•VOUT 为模块的输出电压，单位为 V

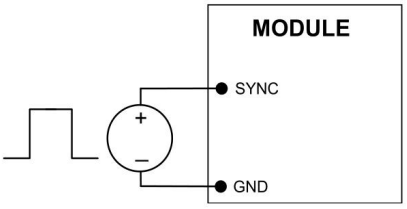
•COUT 为输出电容的总容值，单位为 F

•tSS 为所选的软启动时间，单位为 s

计算出充电电流后，可将过流阈值配置为最大负载电流和输出电容充电电流之和并留一定余量。所需保证的余量可取决于特定的应用场合，但建议为 25%。

注意事项：对于两个模块并联应用时，两个模块的软启动时间必须配置为相同的值。

频率设置、时钟同步 SYNC



模块的开关频率可以同步一个在指定范围内具有外部频率的信号。如上图添加外部时钟信号到模块 SYNC 引脚来完成，其中外来时钟需满足电气规格表指定外部 SYNC 信号要求。

如不使用该引脚，模块应在默认开关频率下运行，且将 SYNC 引脚连接至 GND。

开关频率可以通过 SYNC 引脚上的外部时钟同步。在两模块并联工作时，SYNC 信号的频率必须是开关频率的 4 倍，，SYNC 信号必须是占空比为 50%的方形波形。高电平阈值应大于 2V，低电平阈值应小于 0.8 V。SYNC 和 SHARE2 设置的更改仅在电源重启后生效。

开关机延迟

可通过上位机设置开机延迟时间，可设置输出电压上升时间和关机延迟时间，更多信息可在 PMBus 指令处查阅。

输出电压设置

Trim 引脚连接到内部误差放大器的输入端，内部参考电压为 600 mV±0.5%。

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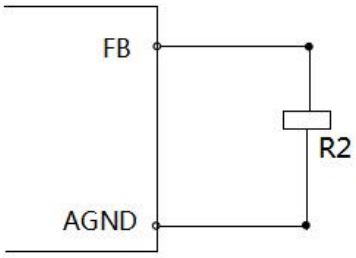

VO(SET)	电阻(kΩ)
0.6	OPEN
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10
3.3	4.4444
4.5	3.0791

$$R2 = R_{FBX}(k\Omega) = \frac{12}{V_O - V_{FB}}$$

模块的输出电压可以使用 VREF_TRIM 命令进行调节，该命令的格式详见 MFR_SPECIFIC_04 (VREF_TRIM) (D4h)说明，其调节范围在输出电压的-20%到 10%之间， VREF_TRIM 命令通常用于精调模块的输出电压，步进为 2mV。另外 MARGINING 和 VREF_TRIM 共同限制了输出电压可调范围在-30%到 10%之间，不建议超过该范围。

KD12S-40A 可以通过以下三种形式确定实际的输出电压：

- No output margin

$$V_{FB} = VREF_TRIM + 0.6$$

- Margin High Voltage State

$$V_{FB} = STEP_VREF_MARGIN_HIGH + VREF_TRIM + 0.6$$

- Margin Low State

$$V_{FB} = STEP_VREF_MARGIN_LOW + VREF_TRIM + 0.6$$

- VTrim 是 Trim 引脚上的电压
- VREF_TRIM 是输出电压的偏置电压
- VREF_MARGIN_HIGH 是输出电压可调的边际电压上限
- VREF_MARGIN_LOW 是输出电压可调的边际电压下限

PGOOD

模块会检测 Trim 引脚上的电压，用于判断输出电压是否在设定值范围内。在软启动过程，PGOOD 被拉至地，在软启动结束后，如果输出电压在 PGOOD 阈值范围内（PG_LOW 至 PG_HIGH 之间），PGOOD 引脚会在 2ms 延迟后释放，当输出电压超出 PGOOD 阈值范围内，PGOOD 会立即拉至地。PGOOD 阈值范围（PG_LOW 和 PG_HIGH）可通过 PMBus 指令 MFR_SPECIFIC_07(PCT_VOUT_FAULT)PG_LIMIT)设置。

PGOOD 为开漏引脚，需外接 10K 电阻。

输出过流保护 OC

输出过流保护上位机可设置两种响应方式，一种为短路自恢复，另一种为短路后模块锁存。短路周期为：7 个周期计数（7 × 模块输出电压上升时间），在两模块并联应用下，二路的过流保护响应跟随一路，两个模块需设置在相同的过流保护响应模式下。

输出欠压/过压保护 VOUT UV/OV

模块检测 Trim 引脚上的电压，用于提供输出过压和输出欠压保护，输出过压阈值和输出欠压阈值都可在 PMBus 指令上设置。

输出欠压保护的方式和过流保护一致。

例如若 IOUT_OC_FAULT_RESPONSE 指令设置响应为自恢复重启，那么在欠压保护响应下也为自恢复重启，另外欠压保护只有在软启动结束后才会开始检测。

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当输出过压保护故障发生时，直到电源重启或 CNTL 切换。当输出过压阈值设置为输出电压的百分比时，只有在软启动结束后才会启用输出过压保护，当输出过压阈值设置为固定值时，输出过压保护持续生效。在两项并联应用下，保证两模块 SHARE1 接入 SHARE1 总线只检测模块 1（主机）的 Trim1 的输出欠压/过压故障，其余通道均不会检测。更多信息可查看 MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h) 和 (E0h) MFR_SPECIFIC_16 (COMM_EEPROM_SPARE) 指令。

输入欠压保护 VIN UV

输入欠压保护也可通过上位机设置，具体可查看 VIN_ON 和 VIN_OFF 指令，默认欠压为电气性能表格中描述，这些指令在两模块并联应用时也需要同步设置。

过温保护 OT

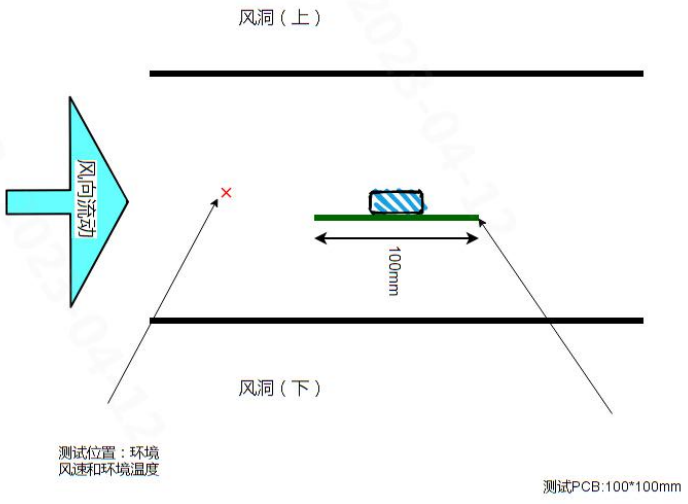
模块内部具有保护功能，上位机同步可修改过温保护点，可设置在 120℃到 160℃之间。

当内部控制 IC 过温故障时（160℃），控制 IC 的 PWM 关闭，当温度下降至 140℃后，PWM 重新启动。

热设计

该产品可工作在不同的热环境下，但必须提供足够的散热以确保模块可靠运行。散热主要通过模块引脚到主板的热传导，以及流经模块的对流风速来实现。该产品有一定程度降额，但不建议过温度使用，温度降额曲线提供了在特定 Vin 下的输出电流与环境温度和风速的关系，具体可见上述表格，测试图见下图。

该模块在 100*100mm 测试板上测试，垂直安装在截面为 300 x 203 mm 的风洞中。另外请注意模块和主板之间连接的低阻抗可有效减少额外的功率损耗。



SHARE1 故障信息

在触发过流、输入欠压、输出过压、输出欠压、过温故障时，SHARE1 引脚会被内部拉低，此外，如果模块的 SHARE1 引脚在外部被拉低，该模块也会关闭。

所以在多相应用下，SHARE1 连接至总线，任何一个通道出现故障 SHARE1 被拉低，其余模块也会跟随关闭，如果故障响应设置为自恢复，则只有在每个通道 SHARE1 均被释放后，才可重新启动。

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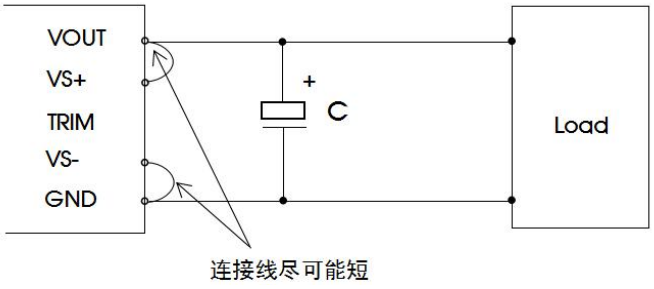
故障信息	输入欠压	过流	输出欠压	输出过压	过温
响应模式	/	可设置自恢复或锁存	可设置自恢复或锁存	锁存	温度低于开启阈值后自恢复
软启动前	开启	关闭	关闭	阈值为固定值时开启/阈值为输出电压百分比时关闭	开启
软启动中	开启	逐周期限流	关闭	阈值为固定值时开启/阈值为输出电压百分比时关闭	开启
软启动后	开启	开启	开启	开启	开启

远端补偿的使用以及注意事项

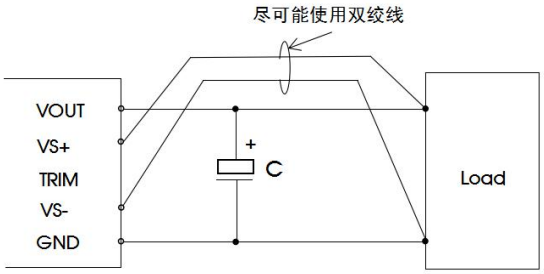
1、当不使用远端补偿时：



注意事项：

1) 当不使用远端补偿时，确保 VOUT 与 VS+，GND 与 VS-短接；
2) VOUT 与 VS+，GND 与 VS-之间的连线尽可能短，并靠近端子。避免形成一个较大的回路面积，当噪声进入这个回路，可能造成模块的不稳定。

2、当使用远端补偿时：



注意事项：

1. 如果使用远端补偿的引线比较长时，可能导致输出电压不稳定，如果必须使用较长的远端补偿引线时请联系我司技术人员。
2. 如果使用远端补偿，请使用双绞线或者屏蔽线，并使引线尽可能短。
3. 在电源模块和负载之间请使用宽 PCB 引线或粗线，并保持线路电压降应低于 0.3V。确保电源模块的输出电压保持在指定的范围内。
4. 引线的阻抗可能造成输出电压振荡或者较大纹波，使用之前请做好足够的评估。

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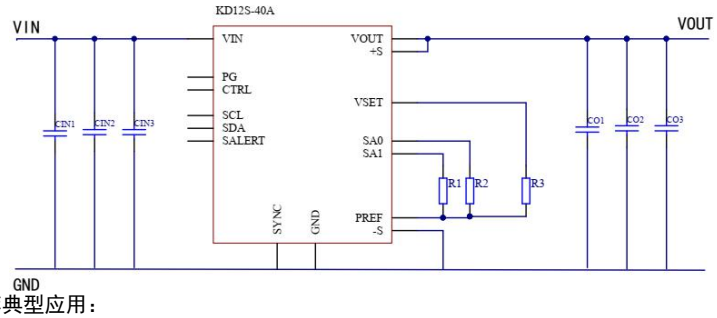
设计参考

典型应用电路

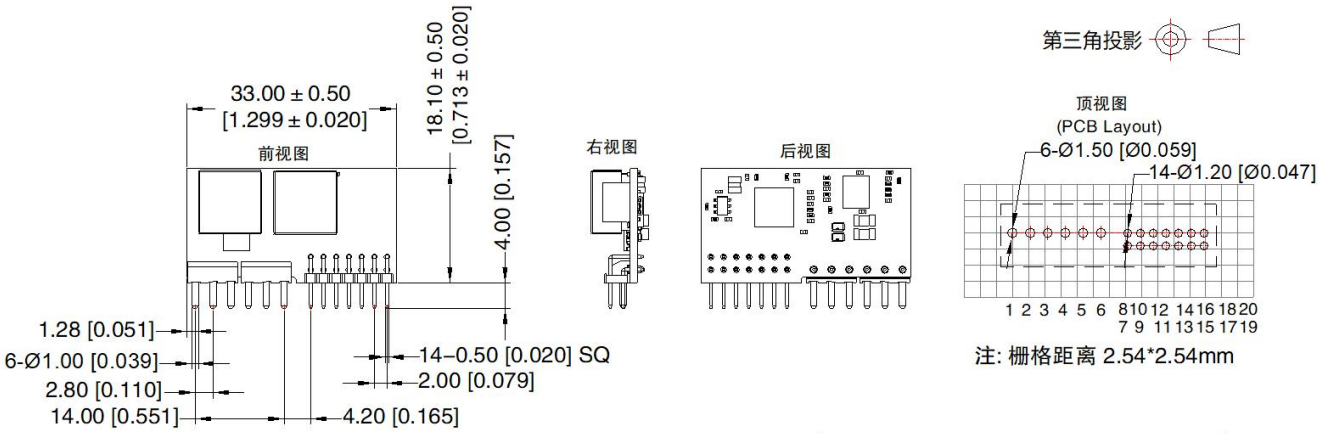
名称		规格
CIN1		2*680uF/35V 电解电容
CIN2		3*22uF/25V 陶瓷电容
CIN3		0.1uF/25V 陶瓷电容
CO1	其他输出	0.1uF/6.3V 陶瓷电容
	3.3V 输出	--
CO2	3.3V 输出	6*47uF/6.3V+1*22uF/10V 陶瓷电容
	其他输出	5*47uF/6.3V+2*22uF/10V 陶瓷电容
CO3	0.6V 输出	1*100uF/25V+3*220uF/25V+1*680uF/35V 电解电容
	3.3V 输出	2*680uF/35V 电解电容
	其他输出	2*220uF/25V+1*680uF/35V 电解电容
R1		OPEN
R2		
R3		30K



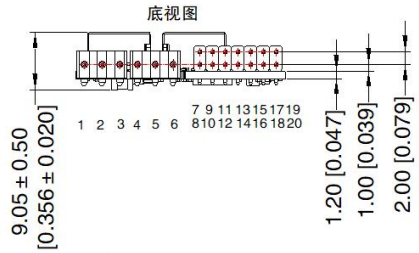
推荐典型应用：

VIN: 12V
VOUT: 1.0V
IOUT: 40A

外观尺寸图



注：栅格距离 2.54*2.54mm



注：
尺寸单位：mm[inch]
端子直径公差：±0.10[±0.004]
未标注公差：±0.25[±0.010]
器件布局仅供参考，具体以实物为准

引脚方式			
引脚	功能	引脚	功能
1	Vin	11	SDA
2	Vin	12	SALERT
3	GND	13	SA1
4	GND	14	SCL
5	Vo	15	SYNC
6	Vo	16	SA0
7	-S	17	CTRL
8	+S	18	PG
9	NC	19	PREF
10	VSET	20	NC

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PMBusg 关键寄存器详情

OPERATION(01h)	该指令用于操作 CNTL（CTRL）来开启或关闭模块，也可用于设置输出电压的精调。 为了访问模块通道 1 的 OPERATION 寄存器，PAGE 必须设置为 0，若为了访问模块通道 2 的 OPERATION 寄存器，PAGE 必须设置为 1，如果要同时访问通道 1 和通道 2，PAGE 必须设置为 11。 如果通道被配置为从机，则该通道无法访问该指令，该指令的任何写入都将被忽略，尝试读写从机通道的任何指令都会报告故障并触发 SMBALERT。
IOUT_CAL_GAIN	IOUT_CAL_GAIN 必须等于实际电感器 DCR 值，以实现精确的电流读数和 OC 故障保护。
Enable and UVLO	ON_OFF_CONFIG 命令用于选择转换器的开启行为。在本示例中，只要输入电压存在且高于 UVLO 阈值，无论操作状态如何，都使用 CTRL 端子来启用或禁用转换器。如果 CTRL 端子悬空，则通过内部 6μA 电流源将其拉至 5V。
TON_RISE	软启动时间命令可设置软启动时间，选择软启动时间时需要考虑输出电容器的充电电流。在某些 应用 （例如具有大量输出电容的应用）中，如果未正确选择软启动时间，那么该电流可能导致错误的过流保护电路跳变。为避免误的跳变，在选择软启动时间和过流阈值时应包括输出电容器充电电流。可以使用公式计算电容器充电电流：$I_{CAP}=\frac{V_{OUT}\times C_O}{t_{ss}}$ 。
IOUT_OC_FAULT_LIMIT	过流阈值和响应令可设置过流阈值。模块使用电感器峰值电流值进行过流检测。应将电流限制设置为最大电感器峰值电流，加上启动期间的输出电容器充电电流，再加上一些负载瞬态和元件变化余量。所需的余量大小取决于各个应用，对于该应用，最大电感器峰值电流为，该设计允许一些额外的余量，因此选择了 50A（峰值电流）的过流阈值。
IOUT_OC_FAULT_RESPONE	IOUT_OC_FAULT_RESPONE 命令可设置所需的过流事件响应。在该示例中，转换器配置为在发生过流情况时进入间断模式。模块还可以配置为在发生过流情况时锁存。

PMBus 详细寄存器

CODE	COMMAND NAME	WORD/BYTE	DESCRIPTION: PMBus Command	USER WRITABLE	FACTORY DEFAULT VALUE
00h	PAGE	Byte	Locates separate PMBus command lists in multiple output environments	YES	0XXX XXX0
01h	OPERATION	Byte	Turn the unit on and off in conjunction with the input from the CONTROL pin. Set the output voltage to the upper or lower MARGIN VOLTAGES.	YES	0X00 00XX
02h	ON_OFF_CONFIG	Byte	Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.	YES	XXX1 0110
03h	CLEAR_FAULTS	Byte	Clears all fault status registers to 0x00. The "Unit is Off" bit in the status byte is not cleared when this command is issued.	YES[1]	NONE
10h	WRITE_PROTECT	Byte	Prevents unwanted writes to the device.	YES	000X XXXX
15h	STORE_USER_ALL	Byte	Saves the current configuration into the User Store. Note: This command writes to Non-Volatile Memory.	YES[1]	NONE
16h	RESTORE_USER_ALL	Byte	Restores Store. all parameters to the settings saved in the User	YES[1]	NONE
19h	CAPABILITY	Byte	PEC,SPD,ALRT	No	1011 0000
20h	VOUT_MODE	Byte	Read-Only Mode Indicator. The data format is linear with an exponent of -9	No	0001 0111
35h	VIN_ON	Word	Sets the value of the input voltage at which the unit should start power conversion	YES	1111 0000 0001 0001
36h	VIN_OFF	Word	Sets the value of the input voltage at which the unit should stop power conversion.	YES	1111 0000 0001 0000

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38h	IOUT_CAL_GAIN	Word	Sets the ratio of the voltage at the current sense pins to the sensed current.	YES	1000 0000 0010 0001
39h	IOUT_CAL_OFFSET	Word	Nulls any offsets in the output current sensing circuit	YES	1110 0000 0000 0000
46h	IOUT_OC_FAULT_LIMIT	Word	Sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition.	YES	1111 1000 0001 1110
47h	IOUT_OC_FAULT_RESPONSE	Byte	Instructs the device on what action to take in response to an output over-current fault.	YES	0000 0111
4Ah	IOUT_OC_WARN_LIMIT	Word	Sets the value of the output current that causes an output Over-current warning	YES	1111 1000 0011 0010
4Fh	OT_FAULT_LIMIT	Word	over-temperature fault threshold	YES	0000 0000 1000 0010
5Ih	OT_WARN_LIMIT	Word	over-temperature warning threshold	YES	0000 0000 01111000
61h	TON_RISE	Word	Target soft-start rise time	YES	1110 0000 0010 1011
78h	STATUS_BYTE	Byte	Single byte status indicator	No	0x00 0000
79h	STATUS_WORD	Word	Full 2-byte status indicator	No	0000 0000 0x00 0000
7Ah	STATUS_VOUT	Byte	Output voltage fault status detail	No	0000 0000
7Bh	STATUS_IOUT	Byte	Output current fault status detail	No	0000 0000
7Dh	STATUS_TEMPERATURE	Byte	Temperature fault status detail	No	0000 0000
7Eh	STATUS_CML	Byte	Communication, memory, and logic fault status detail	No	0000 0000
80h	STATUS_MFR_SPECIFIC	Byte	Manufacturer specific fault status detail	No	0000 0000
8Bh	READ_VOUT	Word	Read output voltage	No	0000 0000 0000 0000
8Ch	READ_IOUT	Word	Read output current	No	1110 0000 0000 0000
8Eh	READ_TEMPERATURE_2	Word	Read off-chip temp sensor	No	1111 0000 0110 0100
98h	PMBUS_REVISION	Byte	PMBus Revision Information	No	0001 0001
D0h	MFR_SPECIFIC_00	Word	User scratch pad	YES	0000 0000 0000 0000
D4h	MFR_SPECIFIC_04	Word	VREF_TRIM	YES	0000 0000 0000 0000
D5h	MFR_SPECIFIC_05	Word	STEP_VREF_MARGIN_HIGH	YES	0000 0000 0001 1110
D6h	MFR_SPECIFIC_06	Word	STEP_VREF_MARGIN_LOW	YES	1111 1111 1110 0010
D7h	MFR_SPECIFIC_07	Byte	PCT_VOUT_FAULT_PG_LIMIT	YES	XXXX XX10
D8h	MFR_SPECIFIC_08	Byte	SWQUENCE_TON_TOFF_DELAY	YES	111X 000X
E0h	MFR_SPECIFIC_16	Word	COMM_EEPROM_SPARE	YES	1011 0001 xxxx x011
E5h	MFR_SPECIFIC_21	Word	IC options	YES	0111 1111 0000 0000
E6h	MFR_SPECIFIC_22	Word	PWM_OSC_SELECT	YES	0000 0000 0000 0001
E7h	MFR_SPECIFIC_23	Word	Paged and Common MASK_SMBALERT	YES	0000 0000 0000 0000
EFh	MFR_SPECIFIC_30	Word	Temperature offset	YES	1111 1000 0000 0000
F0h	MFR_SPECIFIC_32	Word	API options	YES	0000 0000 0000 0000
FCh	MFR_SPECIFIC_44	Word	Device code, unique code to id part number	No	0000 0001 1110 0000

NOTE 1：No data bytes are sent, only the command code is sent.

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PAGE(00h)

Format	Unsigned binary integer
Description	The PAGE command provides the ability to configure, control, and monitor through only one physical address both channels (outputs) of the device.
Default	0XXX XXX0 (binary)

PAGE							
r/w	r	r	r	r	r	r	r/w
7	6	5	4	3	2	1	0
PA	X	X	X	X	X	X	P0

Bits	Field Name	Description
7,0	PA,P0	00: (Default) All commands address the first channel. 01: All commands address the second channel. 10: Illegal input-ignore this write, take no action. 11: All commands address both channels. If PAGE = 11, any then read commands point to PAGE0 always.
6:1	X	X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

OPERATION (01h)

Format	Unsigned binary integer
Description	The OPERATION command is used to turn the device output on or off in conjunction with the input from the CNTLx pin (where x = 1 for channel 1 and x = 2 for channel 2). It is also used to set the output voltage to the upper or lower MARGIN levels. OPERATION is a paged register. In order to access OPERATION register for channel 1 of the device, PAGE must be set to 0. In order to access OPERATION register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0X0000XX (binary)

r/w	r	r/w	r/w	r/w	r/w	r	r
7	6	5	4	3	2	1	0
On	0	Margin				X	X

Bits	Field Name	Description
7	On	The On bit is used to enable to IC via PMBus. The necessary condition for this bit to be effective is that the cmd bit in the ON_OFF CONFIG register is set high. However, the cmd bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit cpr in the ON_OFF CONFIG register is low, or c. The bit cpr is high and the CNTL_EN pin is enabled (high or low).
6	0	X: Default
5:2	Margin	If Margin Low is enabled, load the value from the STEP_VREF_MARGIN_LOW command. If Margin High is enabled, load the value from the STEP_VREF_MARGIN_HIGH command. (See PMBus specification for more information) 0000: (Default) Margin Off 0101: Margin Low (Ignore Fault) 0110: Margin Low (Act On Fault) 1001: Margin High (Ignore Fault) 1010: Margin High (Act On Fault) Note: Any values written to read-only registers are ignored.
1:0	X	XX: Default X indicates writes are ignored and reads are 0. Any values written to read-only registers are ignored.

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ON_OFF_CONFIG (02h)

Format	Unsigned binary integer
Description	The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. ON_OFF_CONFIG is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Description	However, note that page 0 (channel 1) fault status bits (and associated smbalert state) should be capable of being cleared by toggling CNTL1 pin even if channel 1 is a slave. If channel 2 is a slave, then CNTL2 pin is disabled but toggling the CNTL1 pin should also clear page 1 (channel 2) fault status bits and related smbalert state. (The is recommendation is to tie together CNTL1 pins of both devices in a multi-phase configuration).
Default	XXX10110 (binary) The default power-up state can be changed using the STORE_USER_ALL command.

			r/w^E	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
X	X	X	pu	cmd	cpr	pol	cpa

Bits	Field Name	Description
7:5	X	X indicates writes are ignored and reads are 0.
4	pu	(Format: binary) Sets the default to either operate any time power is present or for the CTRL to be controlled by CONTROL pin and/or PMBus commands. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up. 0: Device powers up any time power is present regardless of state of the CONTROL pin. 1: (Default) Device does not power up until commanded by the CNTL_EN pin and/or OPERATION command as programmed in bits (3:0) of the ON_OFF_CONFIG register.
3	cmd	(Format: binary) The cmd bit controls how the device responds to commands received via the serial PMBus. This bit is used in conjunction with the 'cpr', 'pu', and 'on' bits to determine start up. 0: (Default) Device ignores the on bit in the OPERATION command. 1: Device responds to the on bit in the OPERATION command, as explained above.
2	cpr	(Format: binary) Set the CNTL_EN pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up. The cpr bit being high is a necessary but not sufficient condition to enable the IC via the CNTL_EN pin: 0: Device ignores the CNTL_EN pin, i.e., CTRL is controlled only by the OPERATION command 1: (Default) The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, and the CNTL_EN pin is active (high or low), and b. The bit cmd in the ON_OFF CONFIG register is low, or c. The bit cmd is high and the bit on in the OPERATION register is high.
1	pol	(Format: binary) Polarity of the CONTROL pin 1: (Default) CONTROL pin is active high 0: CONTROL pin is active low To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect.
0	cpa	(Format: binary) Sets CONTROL pin action when commanding the unit to turn off. 0: (Default) Use the programmed turn-off delay. Note: Any values written to read-only registers are ignored on write and returns a '0' when read.

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CLEAR_FAULTS (03h)

Format	N/A
Description	CLEAR_FAULTS is a paged command. In order to issue this command for channel 1 of the device, PAGE must be set to 0. In order to issue this command for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command simultaneously clears all bits in all status registers in the selected PAGE. At the same time, the device negates (clears, releases) its SMB_ALERT signal output if the device is asserting the SMB_ALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

WRITE_PROTECT (10h)

Format	N/A
Description	The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings. Note: Valid setting of WRITE_PROTECT(7:5) bits disables the RESTORE_USER_ALL command' s ability to restore EEPROM data to protected PMBus Control/Status Registers (CSRs). However, an EEPROM (via the RESTORE_USER_ALL execution) restores the data to any registers the remain unprotected (either by a valid WRITE_PROTECT(7:5) setting, or by any invalid setting of these bits). No WRITE_PROTECT(7:5) bit setting affects the Reset-Restore operation. All registers having EEPROM support get updated. Likewise, STORE_USER_ALL command operation remains unaffected.
Default	000XXXXX (binary) The default power-up state can be changed using the STORE_USER_ALL command.

r/w^E	r/w^E	r/w^E					
7	6	5	4	3	2	1	0
bit7	bit6	bit5	X	X	X	X	X

Bits	Field Name	Description
7	bit7	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)
6	Bit6	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and PAGE commands. (bit5 and bit7 must be 0 to be valid data)
5	Bit5	(Format: binary) 0: (Default) See table below. 1: Disable all writes except for the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands. (bit6 and bit7 must be 0 to be valid data)
4:0	X	X indicates writes are ignored and reads are 0. Note: Any values written to read-only registers are ignored.
Invalid data written to WRITE_PROTECT(7:5) causes the cml bit in the STATUS_BYTE and the ivd bit in the STATUS_CML registers to be set. INVALID DATA ALSO RESULTS IN NO WRITE PROTECTION (WRITE_PROTECT = 00h)!		

Data Byte Value	Action
1000 0000	Disables all WRITES except to the WRITE_PROTECT command.
0100 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, and PAGE commands.
0010 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands.

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STORE_USER_ALL (15h)

Format	N/A
Description	Store all of the current storable register settings in the EEPROM memory as the new defaults on power up. It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the write operation with unpredictable memory storage results. It is recommended to turn the device output off before issuing this command. EEPROM programming faults set the cml bit in the STATUS_BYTE and the oth bit in the STATUS_CML registers.

RESTORE_USER_ALL (16h)

Format	N/A
Description	Write EEPROM data to those registers which: (1) have EEPROM support, and; (2) are unprotected according to current setting of the WRITE_PROTECT(7:5) bits. It is permitted to use the RESTORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. It is recommended to turn the device output off before issuing this command.

Bits	Field Name	Description
7:0		No data bytes are sent, only the command code is sent.

CAPABILITY (19h)

Format	N/A
Description	This command provides a way for a host system to determine some key capabilities of this PMBus device.
Default	10110000 (binary)

r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
PEC	SPD		ALRT	Reserved			

Bits	Field Name	Description
7	PEC	(Format: binary) Packet Error Checking is supported. 1: Default Note: Any values written to read-only registers are ignored.
6:5	SPD	(Format: binary) Maximum supported bus speed is 400 kHz. 01: Default Note: Any values written to read-only registers are ignored.
4	ALRT	(Format: binary) This device does have a SMB_ALERT pin and does support the SMBus Alert Response Protocol. 1: Default Note: Any values written to read-only registers are ignored.
3:0	Reserved	Reserved bits. 0000: Default

VOUT_MODE (20h)

Format	N/A
Description	The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below. If a host sends a VOUT_MODE writer command, the device rejects the VOUT_MODE command, declare a communication fault for invalid data and respond as described in PMBus specification II section 10.2.2.
Default	00010111 (binary)

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r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
Mode			Exponent				

Bits	Field Name	Description
7:5	Mode	(Format: binary) 000: (Default) Linear Format
4:0	Exponent	(Format: two's SHARE3lement binary) 10111: (Default) Exponent value = - 9 Note: Any values written to read-only registers are ignored.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start power conversion assuming all other conditions are met.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4.25(default)	4.5	4.75	5	5.25	5.5	5.75
6	6.25	6.5	6.75	7	7.25	7.5
7.75	8	8.25	8.5	8.75	9	9.25
9.5	10	10.5	11	11.5	12	12.5
13	14	15	16			

Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data - in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_ON remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_ON should not attempt to set its value less than that of VIN_OFF.
Default	The default setting results in a real VIN_ON of 4.25 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11110 (bin) - 2 (dec) (equivalent LSB = 0.25 V) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the Mantissa for the linear format. Default: 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25 V) Minimum: 000 0001 0001 (bin) 17 (dec) (equivalent VIN_ON voltage = 4.25 V) Maximum: 000 0100 0000 (bin) 64 (dec) (equivalent VIN_ON voltage = 16 V) Note: Any values written to read-only registers are ignored

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop power conversion.

Values written within the supported VIN range are mapped to the nearest supported increment.

The supported VIN_ON values are:

4(default)	4.25	4.5	4.75	5	5.25	5.5
5.75	6	6.25	6.5	6.75	7	7.25
7.5	7.75	8	8.25	8.5	8.75	9
9.25	9.75	10.25	10.75	11.25	11.75	12.25
12.75	13.75	14.75	15.75			

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Format	Linear
Description	Attempts to write values outside of the acceptable range are treated as invalid data – in effect, the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register are set, and SMB_ALERT asserted. Additionally, the value of VIN_OFF remains unchanged. Maintaining values within "acceptable range" also indicates that writes to VIN_OFF should not attempt to set its value equal to or higher than that of VIN_ON.
Default	The default setting results in a real VIN_OFF of 4 V The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11110 (bin) –2 (dec) These default settings are not programmable. Note: Any values written to read-only registers are ignored
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the linear format Mantissa. Default: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4 V) Minimum: 000 0001 0000 (bin) 16 (dec) (equivalent VIN_OFF voltage = 4 V) Maximum: 000 0011 1111 (bin) 63 (dec) (equivalent VIN_OFF voltage = 15.75 V) Note: Any values written to read-only registers are ignored.

IOUT_CAL_GAIN (38h)

Format	Linear
Description	The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are ohms. The effective current sense element is the DCR of the inductor. The default setting is 0.5 mΩ. The resolution is 15.26 μΩ. The range is 0.244 to 7.747 mΩ. The IOUT_CAL_GAIN needs to be set to 0.5 mΩ for correct current readout. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1), PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE 0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. IOUT_CAL_GAIN is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the device , PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11
Default	The default setting results in a real IOUT_CAL_GAIN of 0.5035 mΩ. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

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Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 10000 (bin) – 16 (dec) (15.26μΩ) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the linear format Mantissa. Default: 000 0010 0001 (bin) 32 (dec) (32×15.26μΩ = 0.5035 mΩ) Minimum 016 (dec) = 16×15.26 μΩ = 0.244 mΩ Maximum 508 (dec) = 508× 15.26 μΩ = 7.747 mΩ Note: Any values written to read-only registers are ignored.

IOUT_CAL_OFFSET (39h)

Format	Linear
Description	The IOUT_CAL_OFFSET is used to SHARE3ensate for offset errors in the READ_IOUT command, the IOUT_OC_FAULT_LIMIT command and the IOUT_OC_WARN_LIMIT command. The units are amps. The default setting is 0 A. The resolution is 62.5 mA. The range is 3.9375 A to -4 A. Values outside the valid range are not checked and become aliased into the valid range. For example, 1110 0100 0000 0001 has an expected value of – 63.9375 A but results in 1110 0111 1111 0001 which is – 3.9375 A. This change occurs because the read-only bits are fixed. The exponent is always –4 and the 5 msb bits of the mantissa are always equal to the sign bit. IOUT_CAL_OFFSET is a paged register. In order to access this register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access this register for channel 2 of the controller, PAGE(7),(0) must be set to 01. For simultaneous access of channels 1 and 2, PAGE(7),(0) command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (i.e. the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value are used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11100 (bin) –4 (dec) (lsb = 62.5 mA) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the linear format Mantissa. This is the linear format Mantissa. Default: 0 (bin) 0 (dec) Bits 1:0, and 7:6 changes for sign extension but are not otherwise programmable Note: Any values written to read-only registers are ignored.

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IOUT_OC_FAULT_LIMIT (46h)

Format	Literal
Description	The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an over-current fault condition. The IOUT_OC_FAULT_LIMIT should always be set to equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the ’ cml’ bit in the STATUS_BYTE register and the ‘ivd’ bit in the STATUS_CML registers and assert SMB_ALERT. IOUT_OC_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK’d command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1000 0011 0010 (binary) The default setting results in a real IOUT_OC_FAULT_LIMIT of 25 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two’s SHARE3lement) This is the exponent for the linear format. Default: 11111 (bin) -1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two’s SHARE3lement) Default: 000 0011 0010 (bin) 50 (dec) (equivalent analog OC = 25 A) Minimum: 000 0000 0110 (bin) 6 (dec) (equivalent analog OC = 3 A) Maximum: 000 0110 0100 (bin) 100 (dec) (equivalent analog OC = 50 A) Note: Any values written to read-only registers are ignored.

IOUT_OC_FAULT_RESPONSE (47h)

Format	Unsigned binary
Description	The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT or a VOUT under-voltage (UV) fault. When an OC fault is triggered, the device also: • Sets the OCF bit in the STATUS_BYTE register • Sets the OCFW and OCF bits in the STATUS_WORD register • Sets the OCF and OCW bits in the STATUS_IOUT register • Asserts SMB_ALERT, and notifies the host as described in section 10.2.2 of the PMBus Specification. Bits (2:0) are hard-wired to 0x7 (3’b111) to indicate the 7xSoft-start time delay units in response to an over current or Vout under-voltage fault. IOUT_OC_FAULT_RESPONSE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK’d command and the reporting of an IVC fault and triggering of SMB_ALERT.

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Default	0000 0111 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r/wE	r/wE	r/wE	r	r	r
7	6	5	4	3	2	1	0
0	0	RS(2)	RS(1)	RS(0)	1	1	1

Bits	Field Name	Description
7:6	0	Default: XX (X indicates writes are ignored and reads are 0) Note: Any values written to read-only registers are ignored.
5:3	RS(2:0)	(Format: binary) Output over current retry setting 000:(Default) A zero value for the Retry Setting indicates that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.). 111: A one value for the Retry Setting indicates that the unit goes through a normal startup (Wait → SoftStart) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. Any value other than 000 or 111 is not accepted, such and attempt causes the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML register to be set, and SMB_ALERT to be asserted.
2:0	1	Default: xxx (x indicates writes are ignored and reads are 1) Note: Any values written to read-only registers are ignored.

IOUT_OC_WARN_LIMIT (4Ah)

Format	Literal (5-bit two's SHARE3lement exponent, 11-bit two's SHARE3lement mantissa)
Description	The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition by setting the OCW in bit-5 of the STATUS_IOUT register. • Sets the OTHER bit in the STATUS_BYTE register • Sets the OCFW bit in the STATUS_WORD register • Set the OCW bit in the STATUS_IOUT register • Notifies the host (Asserts SMB_ALERT) IOUT_OC_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the K12DT-60A device, PAGE must be set to 0. In order to access this register for channel 2 of the K12DT-60A controller, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The IOUT_OC_WARN_LIMIT should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	1111 1000 0010 1110 (binary) The default setting results in a real IOUT_OC_WARN_LIMIT of 23 A. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

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Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11111 (bin) －1 (dec) (0.5 A) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the Mantissa for the linear format. Output over current retry setting Default: 000 0010 1110 (bin) 46 (dec) (analog OC Warning = 23 A) Minimum: 000 0000 0100 (bin) 4 (dec) (equivalent analog OC = 2 A) Maximum: 000 0110 0010 (bin) 98 (dec) (equivalent analog OC = 49 A) Note: Any values written to read-only registers are ignored.

OT_FAULT_LIMIT (4Fh)

Format	Literal (5-bit two's SHARE3 lement exponent, 11-bit two's SHARE3 lement mantissa)
Description	The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition when the sensed temperature from the external sensor exceeds this limit. Upon triggering the over-temperature fault, the following actions are taken: • Set the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Set the OTF and OTW bits in the STATUS_TEMPERATURE register • Notify the host (Asserts SMB_ALERT) • Generate internal signal/s CHx_TSD that eventually shut down the gate drivers. OT_FAULT_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device , PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 10000010 (binary) The default setting results in a real OT_FAULT_LIMIT of 130° C. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (represents mantissa with steps of 1° C) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the Mantissa for the linear format. Default: 000 10000010 (bin) 130 (dec) (130° C) Minimum: 000 0111 1000 (bin) 120 (dec) (120° C) Maximum: 000 1010 0101 (bin) 165 (dec) (165° C) Note: Any values written to read-only registers are ignored.

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Table. OT_FAULT THRESHOLD Settings

TEMPERATURE (°C)(1)	OT_FAULT_THRESHOLD (°C BIN)	TEMPERATURE (°C)	OT_FAULT RESET THRESHOLD (°C BIN)
120	01111000	100	01100100
125	01111101	105	01101001
130	10000010	110	01101110
135	10000111	115	01110011
140	10001100	120	01111000
145	10010001	125	01111101
150	10010110	130	10000010
155	10011011	135	10000111
160	10100000	140	10001100
165	10100101	145	10010001

(1) Lists only multiples of 5° C; but, the actual LSB is 1°C.

OT_WARN_LIMIT (51h)

Format	Literal (5-bit two's SHARE3lement exponent, 11-bit two's SHARE3lement mantissa)
Description	The OT_WARN_LIMIT command sets the value of the temperature, in degrees Celcius, which causes an over-temperature warning condition. • Sets the OTFW bit in the STATUS_BYTE register and STATUS_WORD register • Sets the OTW bit in the STATUS_TEMPERATURE register • Notifies the host (Asserts SMB_ALERT) OT_WARN_LIMIT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: PAGE 0 can always be written to. PAGE 1 can be written only if it is a master (in effect, you can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT. The OT_WARN_LIMIT should always be set to less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than OT_FAULT_LIMIT causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers and assert SMB_ALERT.
Default	0000 0000 01111000 (binary) The default setting results in a real OT_WARN_LIMIT of 120° C. The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 00000 (bin) 0 (dec) (1° C) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the Mantissa for the linear format. Default: 000 01111000 (bin) 120 (dec) (120° C) Minimum: 000 0110 0100 (bin) 100 (dec) (100° C) Maximum: 000 1000 1100 (bin) 140 (dec) (140° C) Note: Any values written to read-only registers are ignored.

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Table. OT_WARN_LIMIT Settings

TEMPERATURE (°C)(1)	OT_FAULT_THRESHOLD (°C BIN)	TEMPERATURE (°C)	OT_FAULT RESET THRESHOLD (°C BIN)
100	01100100	80	1010000
105	01101001	85	1010101
110	01101110	90	1011010
115	01110011	95	1011111
120	01111000	100	1100100
125	01111101	105	1101001
130	10000010	110	1101110
135	10000111	115	1110011
140	10001100	120	1111000

(1) Lists only multiples of 5° C; but, the actual LSB is 1°C.

TON_RISE (61h)

Format	Linear
Description	The TON_RISE command sets the time in ms, from when the reference VREF starts to rise until it reaches the end value. It also determines the rate of transition of the reference VREF (either due to VREF_TRIM or STEP_VREF_MARGIN_HIGH/ STEP_VREF_MARGIN_LOW commands), when this transition is executed during the soft-start state. Values written within the supported range of TON_RISE are mapped to the nearest supported increment. TON_RISE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. With regards to multi-phase operation: The user can always write to PAGE 0 (channel 1). PAGE 1 (channel 2) can be written only if it is a master (in effect, the user can not write PAGE 1 if it is configured as a slave). In this case where PAGE 1 is a slave, the PAGE0 value is used for PAGE1/channel 2. Additionally, for 3-phase or 4-phase mode, the second IC PAGE 0 slave must be programmed by the user to have the same limit value as the master in IC 1 (in effect, the burden is on the user and can not be enforced by the hardware). An attempt to write a PAGE 1 (channel 2) SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	The default setting results in TON_RISE of 2.7ms The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 μs) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) This is the Mantissa for the linear format. Default: 000 0110 0000 (bin) 43 (dec) (equivalent to 6 ms) Minimum: Any value equal or less than 12 dec is equivalent to the min 600 μs Maximum: Any value greater than 120 dec is equivalent to 9 ms Note: Any values written to read-only registers are ignored.

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Table . Allowable TON_RISE Values

TON_RISE TIME (ms)	MANTISSA (BINARY)
0.6	000 0000 1010
0.9	000 0000 1110
1.2	000 0001 0011
1.8	000 0001 1101
2.7	000 0010 1011
4.2	000 0100 0011
6	000 0110 0000
9	000 1001 0000

STATUS_BYTE (78h)

Format	Unsigned binary
Description	The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. STATUS_BYTE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults – OVF, UVF, PGOOD are only be set for that slave's master (which may be in the other IC for 3-ph and 4-ph systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_BYTE register also reports communication faults in the Other Faults bit.
Default	0x000000 (binary)

7	6	5	4	3	2	1	0
0	OFF	OVF	OCF	VIN_UV	OTFW	cml	oth

Bits	Field Name	Description
7	0	Default: 0
6	OFF	(Format: binary) Output is OFF This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Unit is on 1: Unit is off
5	OVF	(= VOUT_OV in PMBus Specification) (Format: binary) Output Over-Voltage Fault Triggers SMB_ALERT. For a slave configuration, this bit is set to 0. 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
4	OCF	(=IOUT_OC in PMBus Specification) (Format: binary) Output Over-Current Fault 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
3	VIN_UV	(Format: binary) Input voltage (VIN) under-voltage fault. This bit is defined only on PAGE0. For PAGE1, this bit is 0. This bit is masked before soft-start is finished. 0: (Default) An input under-voltage fault has not occurred. 1: An input under-voltage fault has occurred.

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2	OTFW	(= TEMPERATURE in PMBus Specification) (Format: binary) Over-Temperature Fault/warning OTF or OTW input has been asserted by the external sensor for that channel. 0: (Default) An over-temperature fault or warning has not occurred. 1: An over-temperature fault or warning has occurred.
1	cml	(= CML in PMBus Specification) (Format: binary) Communications, memory or logic fault has occurred. This bit is used to flag communications, memory or logic faults. 0: (Default) A communications, memory or logic fault has not occurred 1: A communications, memory or logic fault has occurred
0	oth	(= NONE OF THE ABOVE in the PMBus Specification) (Format: binary) Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits (7:1) in this register. 0: (Default) A fault or warning not listed in bits (7:1) has not occurred. 1: A fault or warning not listed in bits (7:1) has occurred.

STATUS_WORD (79h)

Format	Unsigned binary
Description	The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. STATUS_WORD is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. If PAGE command is set to 11, then PAGE 0 of the status register is read. The STATUS_WORD also reports a power good fault. If configured as a master, each channel indicates faults on its own channel. However, if configured as a slave, the output voltage faults (OVF, UVF, PGOOD) are be set only for that slave' s master (which may be in the other device for 3-phase and 4-phase systems) while these faults for the slave are set to 0. Flags related to IOUT and TEMPERATURE (OCF, OCW, OTF, OTW) are set on PAGE 0 for channel 1 and PAGE 1 for channel 2, in all modes. The STATUS_WORD also reports communication faults in the Other Faults bit.
Default	000000000x000000 (binary)

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1
VF	OCFW	0	MFR	PGOOD_Z	0	0	0	0	OFF	OVF	OCF	VIN_UV	OTFW	cml

Bits	Field Name	Description
7	VF	(= VOUT in the PMBus Specification) (Format: binary) Voltage Fault = (OVF + UVF) For slave configurations, this bit is set to 0. 0: (Default) An output voltage fault or warning has not occurred. 1: An output voltage fault or warning has occurred.
6	OCFW	(= IOUT/POUT in the PMBus Specification) (Format: binary) Output Current Fault OR Warning = (OCF + OCW) 0: (Default) An output over-current fault or warning has not occurred. 1: An output over-current fault or warning has occurred.
5	0	Default: 0

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4	MFR	(= MFR in the PMBus Specification) (Format: binary) Internal thermal fault (from bandgap) Thermal shutdown fault for the IC 0: (Default) An internal TSD has not occurred. 1: An internal TSD has occurred.
3	PGOOD_Z	(= POWER_GOOD# in the PMBus Specification) (Format: binary) Power Good Fault (in effect, Power Good Indication - Inverted) The Power Good fault is used to flag when the converter output voltage rises or falls outside of the PGOOD window. If the channel is configured as a slave, this bit are set to "0" (PGOOD_Z is only reflected in the master). 0: (Default) A Power Good fault is not present. 1: Device-channel experiencing a Power Good fault.
2:0	0	Default: 0

The STATUS_WORD low byte is the STATUS_BYTE.

STATUS_VOUT (7Ah)

Format	Unsigned binary
Description	The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The PMBus core is notified of these fault conditions via the 2 input pins labeled OVF and UVF. The PMBus core then communicates these faults to the host through its serial communication channel. STATUS_VOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OVF	0	0	UVF	0	0	0	0

Bits	Field Name	Description
7	OVF	(= VOUT OV Fault in the PMBus Specification) (Format: binary) Output Over-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). 0: (Default) An output over-voltage fault has not occurred. 1: An output over-voltage fault has occurred.
6:5	0	Default: 0
4	UVF	(= VOUT UV Fault in the PMBus Specification) (Format: binary) Output Under-Voltage Fault Set based upon the value stored in MFR_SPECIFIC_07 (D7h). If the channel is configured as a slave this bit are set to 0 (this bit is only reflected in the master). The UV fault indicates only an under-voltage condition at the Trim pin and may not necessarily reflect an over-current situation. However, during an output crowbar short condition, the Trim may sag below the UV threshold level before the current reaches the OC threshold, resulting in a UV fault. If the IOUT_OC_FAULT_RESPONSE register is selected to the retry setting, and the output short is persistent, an over-current fault are triggered for subsequent start-up retry attempts. 0: (Default) An output under-voltage fault has not occurred. 1: An output under-voltage fault has occurred.
3:0	0	Default: 0

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STATUS_IOUT (7Bh)

Format	Unsigned binary
Description	The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The PMBus core is notified of these fault conditions via the inputs OCF and OCW. STATUS_IOUT is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OCF	0	OCW	0	0	0	0	0

Bits	Field Name	Description
7	OCF	(= IOUT OC Fault in the PMBus Specification) (Format: binary) Output Over-Current Fault Set based upon the value stored in IOUT_OC_FAULT_LIMIT 0: (Default) An output over-current fault has not occurred. 1: An output over-current fault has occurred.
6	0	Default: 0
5	OCW	(= IOUT OC Warning in the PMBus Specification) (Format: binary) Output Over-Current Warning Set based upon the value stored in IOUT_OC_WARN_LIMIT. 0: (Default) An output over-current warning has not occurred. 1: An output over-current warning has occurred.
4:0	0	Default: 0

STATUS_TEMPERATURE (7Dh)

Format	Unsigned binary
Description	The STATUS_ TEMPERATURE command returns one byte of information relating to the status of the converter's die temperature related faults. STATUS_TEMPERATURE is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
OTF	OTW	0	0	0	0	0	0

Bits	Field Name	Description
7	OTF	(= OT Fault in the PMBus Specification) (Format: binary) Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	(= OT Warning in the PMBus Specification) (Format: binary) Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5:0	0	Default: 0

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STATUS_CML (7Eh)

Format	Unsigned binary
Description	The STATUS_ CML command returns one byte containing PMBus serial communication faults.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
ivc	ivd	pec	mem	0	0	oth	0

Bits	Field Name	Description
7	ivc	(= Invalid/Unsupported Command in the PMBus Specification) (Format: binary) Invalid or unsupported Command Received 0: (Default) Invalid or unsupported Command not Received. 1: Invalid or unsupported Command Received. An attempt to write an invalid PAGE 1 SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
6	ivd	(= Invalid/Unsupported Data in the PMBus Specification) (Format: binary) Invalid or unsupported data Received 0: (Default) Invalid or unsupported data not Received. 1: Invalid or unsupported data Received.
5	pec	(= Packet Error Check Failed in the PMBus Specification) (Format: binary) Packet Error Check Failed This is a CRC byte sent at the end of each data packet. It is implemented as CRC(x) = x8 + x2 + x1 + 1 0: (Default) Packet Error Check Passed 1: Packet Error Check Failed
4	mem	(= Memory Fault Detected in the PMBus Specification) (Format: binary) Memory Fault Detected This bit indicates a fault with the internal memory. 0: (Default) No fault detected 1: Fault detected
3:2	0	Default: 0
1	oth	(= Other Communication Fault in the PMBus Specification) (Format: binary) Other Communication Fault 0: (Default) A communication fault other than the ones listed in this table has not occurred. 1: A communication fault other than the ones listed in this table has occurred.
0	0	Default: 0

STATUS_MFR_SPECIFIC (80h)

Format	Unsigned binary
Description	The STATUS_ MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings.
Default	00000000 (binary)

7	6	5	4	3	2	1	0
otfi	x	x	ivaddr	ch1_sps_SHARE 1	ch2_sps_SHARE 1	ch1_slave	ch2_slave

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Bits	Field Name	Description
7	otfi	(Format: binary) Over temperature fault internal. This bit is required to distinguish an over temperature fault internal to the device from an external temperature fault. 0: (Default) The internal temperature is below the fault threshold. 1: The internal temperature is above the fault threshold.
6:5	x	Default: 0
4	ivaddr	(Format: binary) Invalid PMBus address This bit is set when the PMBus address detection circuit does not resolve to a valid address. In this event, the device responds to the address: 127d. 0: (Default)
3	ch1_sps_SHARE 1	(Format: binary) Channel 1 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
2	ch2_sps_SHARE 1	(Format: binary) Channel 2 smart power-stage fault This bit reports that the smart power-stage has declared a fault (either over-current or over-temperature) . 0: (Default)
1	ch1_slave	(Format: binary) Channel 1 Slave This bit is set when channel 1 is configured as a slave channel (by pulling Trim1 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)
0	ch2_slave	(Format: binary) Channel 2 Slave This bit is set when channel 2 is configured as a slave channel (by pulling Trim2 > 2.5 V before power-up). It is only used for internal read purposes and does not trigger SMBLERT. 0: (Default)

READ_VOUT (8Bh)

Format	Linear
Description	The READ_VOUT command returns two bytes of data in the linear data format that represent the output voltage. The exponent is set to －9 by VOUT_MODE. VOUT = Mantissa x $2^{Exponent}$ READ_VOUT is a paged register. In order to access READ_VOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_VOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE register cannot be set to 11 for READ_VOUT command.
Default	0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Mantissa															

Bits	Field Name	Description
7：0	Mantissa	(Format: unsigned binary) This is the Mantissa for the linear format. Default: 0000 0000 0000 0000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

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READ_IOUT (8Ch)

Format	Linear
Description	The READ_IOUT command returns the output current in amps for each channel. The reading from the Measurement System must be manipulated in order to convert the measured value into the desired value (IOUT). Note: only positive currents are reported. Any SHARE3uted negative current (For example, 0 measured current and －4 A IOUT_CAL_OFFSET) is reported as 0 A. READ_IOUT is a paged register. In order to access READ_IOUT register for channel 1 of the device, PAGE(7),(0) must be set to 00. In order to access READ_IOUT register for channel 2 of the device, PAGE(7),(0) must be set to 01. PAGE(7),(0) register cannot be set to 11 for READ_IOUT command.
Default	E0000h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7：3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11100 (bin) -4 (dec) (62.5 mA lsb) These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) Default: 000 00000000 (bin) 0 (dec) Note: Any values written to read-only registers are ignored.

READ_TEMPERATURE_2 (8Eh)

Format	Linear
Description	The READ_TEMPERATURE_2 command returns the temperature in degrees Celsius of the current channel specified by the PAGE command.
Default	F064h

r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11110 (bin) －2 (dec) 0.25° C These default settings are not programmable. Note: Any values written to read-only registers are ignored.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) Default: 000 0110 0100 (bin) 100 (dec) Note: Any values written to read-only registers are ignored.

PMBus_REVISION (98h)

Format	Linear
Description	The PMBus_REVISION command returns the revision of the PMBus to which the device is SHARE3liant. The device is SHARE3liant to revision 1.1 of the PMBus specification.
Default	00010001b

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

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Bits	Field Name	Description
7:0	/	/

MFR_SPECIFIC_00 (D0h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_00 register is dedicated as a user scratch pad
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0		

MFR_SPECIFIC_04 (VREF_TRIM) (D4h)

Format	Linear
Description	The VREF_TRIM command is used to apply a fixed offset voltage to the reference voltage. VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_x) × 2 mV The maximum trim range is 10% / - 20% of nominal VREF (600 mV) in 2-mV steps. Permissible values are from 60 mV to - 120 mV. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to - 180 mV. If the commanded VREF_TRIM is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. The VREF_TRIM has two data bytes formatted as two’s SHARE3lement binary integer and can have positive and negative values. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command is ignored. (In analog, the master programmed value are used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command, or when in AVS mode results in a NACK’d command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000h (Fixed Offset Voltage = 0 V) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) (sign extended) Bits 6:0 changes for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: binary) Default: 0000 0000 (bin) 0 (dec) 0 mV Minimum: 1100 0100 (bin) –60 (dec) (–120 mV) (sign extended, twos SHARE3liment) Maximum: 0001 1110 (bin) 30 (dec) (60 mV) Bits 7:6 changes for sign extension but are not otherwise programmable

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MFR_SPECIFIC_05 (STEP_VREF_MARGIN_HIGH) (D5h)

Format	Linear
Description	The STEP_VREF_MARGIN_HIGH command is used to increase the value of the reference voltage by shifting the reference higher. When the OPERATION command is set to Margin High, the reference increases by the voltage (in mV) indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VREF_MARGIN_HIGH) × 2 mV The maximum range is 0 to 10% (60 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to －180 mV. If the commanded STEP_VREF_MARGIN_HIGH is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF are set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital). An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	0000 0000 0001 1110 (binary) The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 0000 0000 (bin) Minimum: 0000 0000 (bin) Maximum: 0000 0000 (bin) Note: Any values written to read-only registers are ignored.
7:0	Low Byte	(Format: binary) This specifies a positive offset voltage on to default VREF. Default: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent) Minimum: 0000 0000 (bin) 0 (dec) (0 mV) Maximum: 0001 1110 (bin) 30 (dec) (60 mV = 10% percent)

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MFR_SPECIFIC_06 (STEP_VREF_MARGIN_LOW) (D6h)

Format	Linear
Description	The STEP_VREF_MARGIN_LOW command is used to decrease the reference voltage by shifting the reference lower. When the OPERATION command is set to Margin Low, the output decreases by the voltage indicated by this command. Thus, the changed reference is given by: VREF = 600 mV + (VREF_TRIM + STEP_VOUT_MARGIN_LOW) × 2 mV .The maximum range is 0 to - 20% (- 120 mV) of nominal VREF (600 mV) in 2mV steps. Including settings from both VREF_TRIM and STEP_VREF_MARGIN_x commands, the net permissible range of VREF is 60 mV to - 180 mV. If the commanded STEP_VREF_MARGIN_LOW is outside its valid range, then that value is not accepted; it also causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, and triggers SMB_ALERT. If the combined VREF set by VREF_TRIM and/or STEP_VREF_MARGIN_x is outside the acceptable range, it causes the device to set the cml bit in the STATUS_BYTE register and the ivd bit in the STATUS_CML registers, it triggers SMB_ALERT, and the VREF is set to the highest or lowest allowed value (based on the commanded level). The VREF transition occurs at the rate determined by the TON_RISE (61h) command if the transition is executed during soft-start. Any transition in VREF after soft-start occurs at the rate determined by the highest programmable TON_RISE of 9 ms. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	1111 1111 1110 0010 (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r*	r*	r*	r*	r*	r*	r*	r*	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0	High Byte	(Format: binary) Default: 1111 1111 (bin) (msb is sign bit) Minimum: 1111 1111 (bin) (sign extended) Maximum: 0000 0000 (bin) Bits 6:0 can change for sign extension but are not otherwise programmable
7:0	Low Byte	(Format: two's SHARE3lement) This specifies a negative offset voltage on to default VREF. Default: 1110 0010 (bin) -30 (dec) (–60 mV = –10% percent) Minimum: 1100 0100 (bin) -60 (dec) (–120 mV = –20% percent) Maximum: 0000 0000 (bin) 0 (dec) (0 mV) Bits 7:6 can change for sign extension but are not otherwise programmable

MFR_SPECIFIC_07 (PCT_VOUT_FAULT_PG_LIMIT) (D7h)

Format	Unsigned binary integer
Description	The PCT_VOUT_FAULT_PG_LIMIT is to set the PGOOD, VOUT_UV and VOUT_OV limits. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. (In analog, the master programmed value is used in a multi-phase system. No special action needed from digital.) An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	XXXX XX10 (binary) The default power-up state can be changed using the STORE_USER commands.

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r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	PG(1:0)

Bits	Field Name	Description
7:2	X	X indicates writes are ignored and reads are 0
1:0	PG(1:0)	(Format: binary) PG, UV, OV Limit Selection. Default: 10

Table lists the over-voltage, under-voltage, and power-good threshold voltages. Bit (13) of MFR_SPECIFIC_16 (E0h) register determines the overvoltage setting.

Table. OV, UV, PGOOD Threshold Values

PG(1)	PG(0)	UV_fault (%)	PG_low (%)	PG_high (%)	OV_fault		OV SETTING
					(%)	(mV)	
0	0	- 16.8	- 12.5	12.5	16.8	n/a	Tracking
0	1	- 12.0	- 7.0	7.0	12.0		
1	0	-29.0	- 23.0	7.0	16.8		
1	1	- 29.0	- 23.0	7.0	12.0		
0	0	- 16.8	- 12.5	12.5	N/A	800	Fixed
0	1	- 12.0	- 7.0	7.0		700	
1	0	- 29.0	- 23.0	7.0		800	
1	1	- 29.0	- 23.0	7.0		700	

MFR_SPECIFIC_08 (SEQUENCE_TON_TOFF_DELAY) (D8h)

Format	Unsigned binary integer
Description	The SEQUENCE_TON_TOFF_DELAY command is used to set the delay for turning on the device and the delay for turning off the device as a ratio of TON_RISE. This is a paged register. In order to access this register for channel 1 of the device, PAGE must be set to 0. In order to access this register for channel 2 of the device, PAGE must be set to 1. For simultaneous access of channels 1 and 2, PAGE command must be set to 11. If the channel is configured as a SLAVE, this command can not be accessed for that channel. Any writes to the SLAVE channel for this command are ignored. In such a case, internally the TON_DELAY is set to the minimum value of 50 μs and TOFF_DELAY is set to zero (overriding any contents of EEPROM). An attempt to read and write the SLAVE channel command results in a NACK'd command and the reporting of an IVC fault and triggering of SMB_ALERT.
Default	111X 000X (binary) The default power-up state can be changed using the STORE_USER commands.

r/w^E	r/w^E	r/w^E	r	r/w^E	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0
TON_DEL<2:0>			X	TOFF_DEL<2:0>			X

Bits	Field Name	Description
7:5	TON_DEL<2:0>	(Format: binary) Default: 111b TON_DELAY = TON_RISE × TON_DEL<2:0> This parameter controls the delay from when ON = 1 until soft-start sequence begins. The default value is 18.9 ms. (Start the VOUT ramp without delay)
4	X	X indicates writes are ignored and reads are 0
3:1	TOFF_DEL<2:0>	(Format: binary) Default: 000b TOFF_DELAY = TON_RISE x TOFF_DEL<2:0> This parameter controls the delay from when ON = 0 until the output is disabled. The default value is 0 ms. (Shut off the output without delay)
0	X	X indicates writes are ignored and reads are 0

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Table . Delay Time Ratios

TON_DEL<2:0> TOFF_DEL<2:0>	DELAY TIME RATIO (MULTIPLE OF TON_RISE)
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

NOTE：

If the device turns off due to a turn-off delay time, any attempt to turn on the device before the turn-off delay time expires should be avoided. The device is available to be turned on only after the turn-off delay time expires and the device has been turned off.

MFR_SPECIFIC_16 (COMM_EEPROM_SPARE)(E0h)

Format	Unsigned binary
Description	This register contains EEPROM backed bits brought out to the top of the digital block IO for possible future use by analog or digital circuits
Default	1011 0001 xxxx x011 (binary) The default power-up state can be changed using the STORE_USER commands.

COMM_EEPROM_SPARE							
r/w^E	r/w^E	r/w^E	r/w^E	r	r	r	r
15	14	13	12	11	10	9	8
PGOOD_DEL_EN	DIS_API_CNT	FIX_OVP_EN	DIS_SSPB				

COMM_EEPROM_SPARE							
r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0

Bits	Field Name	Description
15	PGOOD_DLY_EN	(format: binary, access: read/write) Default: 1b PGOOD Delay Enable This bit, when high, enable 2-ms delay for PGOOD detection during startup.
14	DIS_API_CNT	(format: binary, access: read/write) Default: 0b Disables 3-clock count for API valley active state This bit, when high, disables the 3-clock counter for API valley. When the bit is low, the counting is enabled whereby the API-valley function can remain active only 3 consecutive clock cycles before being inactive for another 3 clocks.
13	FIX_OVP_EN	(Format: binary, access: read/write) Default: 1b Enable fixed output voltage OV protection This bit, when high, enables fixed OV protection circuitry that is active after the BP3 and BP5 voltage comes up. When the bit is low, tracking OV protection is enabled instead and in this case, OV protection is enabled only after the soft-start sequence has SHARE3leted.

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12	DIS_SSPB	(Format: binary, access: read/write) Default: 1b Disable pre-bias initiation after soft-start sequence has SHARE3leted. This bit affects the PWM signal only during prebias startup. When this bit is high, PWM switching begins only if the SHARE3 voltage is higher than the PWM ramp valley. When this bit is low, PWM switching is forced to begin after soft-start sequence has SHARE3leted, even when the SHARE3 voltage is lower than PWM ramp valley.

MFR_SPECIFIC_21 (OPTIONS) (E5h)

Format	Unsigned binary
Description	This register is used for setting user selectable options for the controller.
Default	0111 1111 0000 0000 (binary) The default power-up state can be changed using the STORE_USER commands.

Common/Shared							
r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w
7	6	5	4	3	2	1	0
TCO	CH2_CSGAIN_SEL<2:0>		CH1_CSGAIN_SEL<1:0>		en_adc_cntl	EN_TSNS_SHARE1	EN_SPS
r	r	r	r	r	r	r/w^E	r/w
						SMB_OV	msps_SHARE1

Bits	Field Name	Description
7	TCO	(Format: binary) Default: 0b Temperature SHARE3ensation override 0: OCF, OCW thresholds and current measurements are temp SHARE3ensated 1: Temperature SHARE3ensation is "disabled" TCO is a non-paged bit. Any change on TCO bit is applied to both page 0 and page 1.
6:5	CH2_CSGAIN_SEL<1:0>	(Format: binary) 1:0> Default: 11b Ch2 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 2. For high DCR/L ratios, the user can select lower gains for current-loop stability.
4:3	CH1_CSGAIN_SEL<1:0>	(Format: binary) Default: 11b Ch1 current-share gain select This 2-bit bus is used to select the gain of the current-sharing circuit in channel 1. For high DCR/L ratios, the user can select lower gains for current-loop stability. 00: 50 V/V gain 01: 40 V/V gain 10: 30 V/V gain 11: 20 V/V gain
2	en_adc_ctl	(Format: binary) Default: 1b Enable ADC Control Bit. 0: Disable ADC operation. 1: Enable ADC operation.
1	EN_TSNS_SHARE1	(Format: binary) Default: 1b Enable fault input from Smart power stage This bit, when high, makes the device sensitive to fault communication from the smart power stage. When this bit is low, the device ignores the fault indication from the smart power stage. Whether this bit is high or low, the device performs over temperature protection and declares OT fault when Smart power stage temperature is above the OT fault threshold.

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0	EN_SPS	(Format: binary) Default: 1b（forbid change）
7:2		Note: Any values written to read-only registers are ignored.
1	SMB_OV	(Format: binary) Default: 0b Make SMBALERT an OV fault indicator. This has page 0 scope only (in effect, it is defined only on page 0; the page 1 bit is not used). 0: SMBALERT functions normally 1: SMBALERT reports only OV_FAULT
0	msps_SHARE1	(Format: binary) Default: 0b (PAGE scope) 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(3) / STATUS_MFR_SPECIFIC(2) (corresponding to the CH1_SPS_SHARE1 and CH2_SPS_SHARE1 respectively).

MFR _SPECIFIC_22 (PWM_OSC_SELECT) (E6h)

Format	Unsigned binary
Description	This register is used for setting user selectable PWM phase configuration (sync enable, direction of frequency synchronization pulses - in or out - in a master channel and number of phases) in a multi-phase system.
Default	0001h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
											SYNC_MODE<1:0>		ENSYNC	PHASE	

Bits	Field Name	Description
7:0 7:5		Note: Any values written to read-only registers are ignored.
4:3	SYNC_MODE<1:0>	(Format: binary) Default: 00b Synchronization configuration for the oscillator These bits allow the user to configure the internal PWM oscillator clock in the PWM master channel 1 in one of several operating modes as described below. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then these bits are internally forced to <1:1> indicating that external signals on the SYNC and PHDET pins must override the internal clock and phase zero signals. In a case of slave channel 1, any attempt to write a "0" to either one or both bits are treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Self generated clock with internal phasing, switch positions 1 and 3 01: External clock on SYNC pin, but phasing is internal; switch positions 1 and 3 10: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 1 and 3 11: External clock on SYNC pin and external phase signal on PHDET pin; switch positions 2 and 4 (forced for channel 1 slave)

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2	ENSYNC	(Format: binary) Default: 0b Synchronization enable This bit, when high, enables the synchronization drivers. 0: Synchronization is disabled 1: Synchronization is enabled
1:0	PHASE	(Format: binary) Default: 01b Number of phases in the system (that involves the IC). This pair of bits is used to configure the number of phases in the power-supply system containing the IC. This information is then used inside the PWM oscillator to set the master switching frequency and channel phase angles. 1. To change this value, the user must change this value in the register, save it to the EEPROM and then reboot the device via power down for the new value to take effect. 2. If channel 1 is a slave, then the bit PHASE <1> is internally forced to 1 indicating that only 3-ph or 4-ph modes can be enabled. In such a case of slave channel 1, any attempt to write a "0" to this bit is treated as invalid data – in effect, the 'cml' bit in the STATUS_BYTE register and the 'ivd' bit in the STATUS_CML register are set, and SMB_ALERT asserted. 00: Independent, dual channel operation 01: Two-phase operation (within single IC) 10: Three-phase operation (between two ICs) 11: Four-phase operation (between two ICs)

NOTE:

A 120° phase shift can be achieved between three phases at 3-phase plus 1-phase configuration, the 1-phase rail has the same phase as channel 1 of the master IC.

A 90° phase shift can be achieved between all four phases at all other configurations listed in the table. SYNC pins of two devices need to be connected, and SHARE2 pins of two devices need to be connected.

Table. Phase Configurations(1)

PHASE CONFIGURATIONS	MASTER IC			SLAVE IC		
	SYNC_MODE	ENSYNC	PHASE	SYNC_MODE	ENSYNC	PHASE
3-phase + 1-phase	00	1	10	11	1	10
4-phase	00	1	11	11	1	11
2-phase + 2-phase	00	(2)	11	11	(2)	11
2-phase + dual-output	00	(2)	11	11	(2)	11
Dual-output + dual-output	00	(2)	11	11	(2)	11

(1) For 3-phase plus 1-phase configuration and 4-phase configuration, SYNC_MODE, ENSYNC and PHASE can be programmed, saved to EEPROM at one time and then reboot the device for the new value to take effect.

(2) For all other configurations listed in the table, follow these steps to program two devices to avoid potential damage.

1. Set ENSYNC to 0 on each device.
2. Program SYNC_MODE and PHASE correctly at both devices, save to the EEPROM and then reboot the devices.
3. Set ENSYNC to 1 on each device to enable synchronization between two devices. No reboot is needed.

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MFR_SPECIFIC_23 (MASK SMBALERT) (E7h)

Format	Unsigned binary
Description	The MFR_SPECIFIC_23 (MASK SMBALERT) command may be used to prevent a warning or fault condition from asserting the SMBALERT signal. This command is unique in that it is partially paged; and partially common/shared – since some faults are channel dependent; and others are channel independent. The upper 8 bits of this register always controls and accesses the shared/common set of faults, regardless of the (00h) PAGE setting. However, the control and access for the lower 8 bits of this register are (00h) PAGE dependent and controls or reflects the currently selected page. Only provides below two options for MASK_SMBALERT setting. ● When en_auto_ARA bit (auto Alert Response Address response) is enabled, all other bits in this PMBus register need to be disabled. ● When en_auto_ARA bit is disabled, any other bits in this PMBus register can be set as desired.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

Common/Shared								PAGE0, PAGE1							
r/w	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w	r/w^E	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
motfi	mprtcl_err	msmb_TO_err	mivc	mivd	mpec	mmem	en_auto_ARA	mOTF	mOTW	mOCF	mOCW	mOVF	mUVF	mPGOOD_Z	mVIN_UV

Bits	Field Name	Description
7	motfi	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_MFR_SPECIFIC(7)
6	mprtcl_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB Protocol Error from the PMBus interface module. One of 2 sources is STATUS_CML(1).
5	msmb_TO_err	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of SMB_TIMEOUT from the PMBus interface module. One of 2 sources is STATUS_CML(1).
4	mivc	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(7)
3	mivd	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(6)
2	mpec	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(5)

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1	mmem	(Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_CML(4)
0	en_auto_ARA	(Format: binary) Default: 0b Enables auto Alert Response Address response. When this feature is enabled, the hardware automatically masks any fault source currently set from re-asserting SMB_ALERT when this device responds to an ARA on the PMBus. This prevents PMBus "bus hogging" in the case of a persistent fault in a device that consistently wins ARA arbitration due to its device address. In contrast, when this bit is cleared, immediate re-assertion of SMB_ALERT is allowed in the event of a persistent fault and the responsibility is upon the host to mask each source individually. When WRITE_PROTECT is set to 20h, 40h or 80h, en_auto_ARA is enabled automatically.
7	mOTF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(7)
6	mOTW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_TEMPERATURE(6)
5	mOCF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(7)
4	mOCW	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_IOUT(5)
3	mOVF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(7)
2	mUVF	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_VOUT(4)

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1	mPGOOD_Z	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_WORD(11)
0	mVIN_UV	Functionality of mask bit: (Format: binary) Default: 0b 0: No effect upon SMBALERT 1: Masks SMBALERT assertion due to setting of STATUS_BYTE(3)

MFR_SPECIFIC_30 (TEMP_OFFSET) (EFh)

Format	Unsigned binary
Description	This paged register is used for setting user selectable offset in the measured temperature. The specified offset value is added to the post-math digital output. The new, post-offset, post-averaging temperature is used for READ_TEMP_2 reporting and for temperature SHARE3ensation of IOUT_CAL_GAIN for both reporting READ_IOUT, and OC_FAULT_LIMIT/WARN threshold setting.
Default	F800h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r/w^E	r	r	r	r	r	r	r	r/w^E	r/w^E	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Exponent					Mantissa										

Bits	Field Name	Description
7:3	Exponent	(Format: two's SHARE3lement) This is the exponent for the linear format. Default: 11111 (bin) –1 (dec) (LSB = 0.5 deg) These default settings are not programmable.
2:0 7:0	Mantissa	(Format: two's SHARE3lement) Default: 000 (bin) 0 (dec) (0 deg) Minimum 7F8 = –8 x 0.5 deg = –4 deg Maximum 006 = 6 x 0.5 deg = 3 deg

MFR_SPECIFIC_32 (API_OPTIONS) (F0h)

Format	Unsigned binary
Description	This paged, user-accessible register is used for setting the API SHARE3arator thresholds and other related options.
Default	0000h The default power-up state can be changed using the STORE_USER commands.

r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
										API_VAL_HIGH	API_VAL_EN	API_AVG	API_EN	API_SET<1:0>	

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Bits	Field Name	Description
7:0 7:6		Note: Any values written to read-only registers are ignored.
5	API_VAL_HIGH	(Format: binary) Default: 0b API valley high threshold When this bit is high, the detection threshold for the API valley circuit is increased to approximately 100 mV from the default value of 50 mV.
4	API_VAL_EN	(Format: binary) Default: 0b API valley enable When this bit is high, API valley circuit is enabled to improve load-dump transient response. When the SHARE3 voltage drops suddenly during load-dump and the variation of SHARE3 voltage exceeds the threshold, the API valley function is triggered. As a result, both high-side and low-side switches are turned off to force the load current go through the body diode of low-side switch to reduce output voltage spike.
3	API_AVG	(Format: binary) Default: 0b API average mode When this bit is high, API circuit uses average value of SHARE3 instead of peak value for threshold detection.
2	API_EN	(Format: binary) Default: 0b API enable When this bit is high, API circuit is enabled to improve load step-up transient response. When the SHARE3 voltage goes high suddenly during load step-up and the variation of SHARE3 voltage exceeds the threshold, the API function is triggered. As a result, additional pulses are injected to reduce output voltage dip 0: API is disabled 1: API is enabled
1:0	API_SET<1:0>	(Format: binary) Default: 00b API SHARE3arator threshold setting This is a 2-bit user setting for selecting the appropriate API SHARE3arator threshold. 00: 35 mV 01: 60 mV 10: 85 mV 11: 110 mV

MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)

Format	Unsigned binary
Description	The DEVICE_CODE command returns a 12-bit unique identifier code for the device and a 4-bit device revision code.
Default	01E0h

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r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Bits	Field Name	Description
7:0 7:4	Identifier Code	0000 0001 1110b : Device ID Code Identifier for the device
3:0	Revision Code	0000b : Revision Code (first silicon starts at 0)

注：

1.包装信息请参见《产品出货包装信息》，包装包编号：58220084；
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